

Performance Limitations of B6 Inverters during Unsymmetrical Voltage Sag Conditions

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Abstract. This Paper deals with the performance limitations of B6 inverters when operated under unsymmetrical voltage sags. Three different strategies the IARC, the ICPS and the PNSC will be investigated and conclusions will be drawn as of the required overdimensioning of the converter, optimum control strategy and theoretical compliance of this inverter topology with current Fault-Ride-Through norms.

Key words

Fault-Ride-Through, grid inverter, distributed generation.

1. Introduction

During the last decade, there has been an exponential increase in the amount of Distributed Generation (DG) injected to the grid. One of the concerns derived from this situation is the behaviour of those large DG parks during grid faults. Current grid regulations enforce Wind Turbines (WT) to remain connected to the network through a fault condition and to immediately provide the power when the voltage sag has been cleared. Despite that the regulatory framework only obligates the WT to remain connected, with a growing number of other DG devices being suddenly disconnected from the grid the effect of the voltage sag would grow. That makes compulsory to design a flexible active power controller for such DGs capable of adapting to faults in the grid and reconfigurable in the case of changes in the grid requirements.

As stated by Rodriguez et al. “during unbalance conditions, it is possible to obtain zero active and reactive power oscillations only by accepting highly distorted currents. However, an intermediate solution allows having sinusoidal grid currents compensating for the oscillation in the active power only, while oscillations are present in the reactive one.” [1]. The impact of this statement is enormous on converters connected to Renewable Energy sources, not only because it would allow complying with future Fault-Through regulations

but because of the fact that the source would be able to deliver all of its power to the grid, minimising the use of dump loads, and maximising its Energy Yield. In order to define a flexible active power controller capable of that, different control strategies have been suggested [2]-[7].

The utilisation of these control strategies, although promising, may present a higher loading of the components in the converter, which should be revised in order to prevent premature failure of the inverter. Moreover, the implementation of the proposed techniques might be topology dependent.

From all three phase converters topologies, one of the most common is the Three-Phase, Six-switch Voltage Source Inverter (commonly known as B6-VSI) and also a standard topology in industrial applications [8]; thus its use in medium-power inverters (in the range of 10 kW, 400V) is broadly used.

The aim of this work is to investigate the applicability of two different control strategies from the aforementioned strategies, the IARC (Instantaneous Active Reactive Control) and the PNSC (Positive–Negative-Sequence Control), as well as a control that would emulate a synchronous generator in the B6-VSI. These strategies will be characterised with respect to the following points:

- Theoretical maximum allowed unbalance for maintaining the active output power level to the one before the fault is present.
- Voltage and Current overload of inverter components.
- Maximum active power transfer for the worst case unsymmetrical scenario presented by Fault-Ride-Through norms (if theoretically possible).

From this investigation, conclusions will be drawn as of the required overdimensioning of the converter, control strategy and theoretical compliance of this inverter topology with current Fault-Ride-Through norms.

Although, these norms are not meant to enforce small DG units, there is no specific regulation for that case.

2. Approach

Nowadays, the control of a standard DG unit is based on the Figure 1, which leads to a disconnection based on time.

The work presented in this paper consisted in performing a simulation of the behaviour of the three control strategies described before facing asymmetrical voltage sags without disconnection.

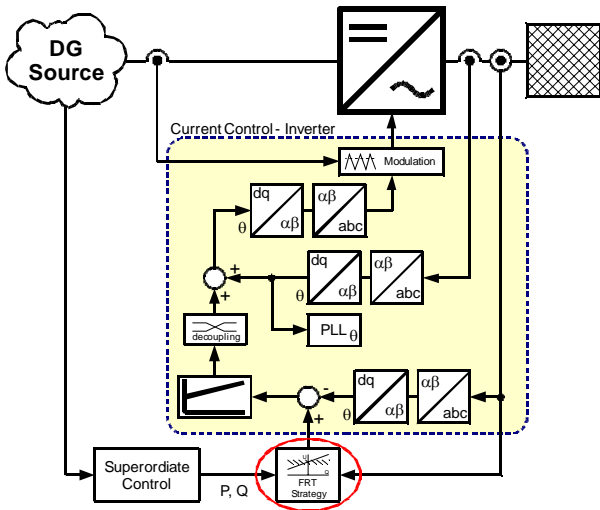


Figure 1: Standard control of a FRT inverter

Figure 1 shows the most generalized control loop of three phase inverters [12]. Enclosed within the circle is the Fault-Ride-Through Control loop, which may, if necessary, take over the superordinate control.

A. Assumptions and Notation

The following sections present results in a per-unit base unless otherwise noted. The base voltage has been defined to be the Line-to-Neutral voltage (as opposed to the common line-to-line voltage) for simplification purposes. Thus the following per unit conversions have been used:

$$i_{base} = \frac{S_{base}}{nV_{base}} \quad (1)$$

$$Z_{base} = \frac{V_{base}^2}{S_{base}} \quad (2)$$

Where n will be defined as the number of phases of the system (n = 1 for one-phase systems and n = 3 for three phase systems)

Any conductance or reactance expressed in percent is referred to as the proportion (in percent) of the base impedance.

Active Power is calculated as the sum of all instantaneous powers on all phases. Reactive Power in

three phase systems is calculated from its alpha and beta components as:

$$Q_{gen} = u_{\alpha}i_{\beta} - u_{\beta}i_{\alpha} \quad (3)$$

Please note that an injection of reactive power ($Q_{gen} < 0$) is in fact a generation of reactive power and thus represented as positive in all graphs.

3. The Topology

This topology, called a B6-Bridge, has three active legs, and even though a neutral line may or may not be connected, it can only inject current in these three legs, making it impossible to inject compensation currents through the Neutral. The topology is a Voltage Source Inverter. Due to the properties of symmetrical three-phase systems, this topology has little DC-Link Capacity requirements, ranging normally in the order around 100 μ F as opposed to the usual 2 mF required by one-phase inverters in the 3 -3.5 kW range.

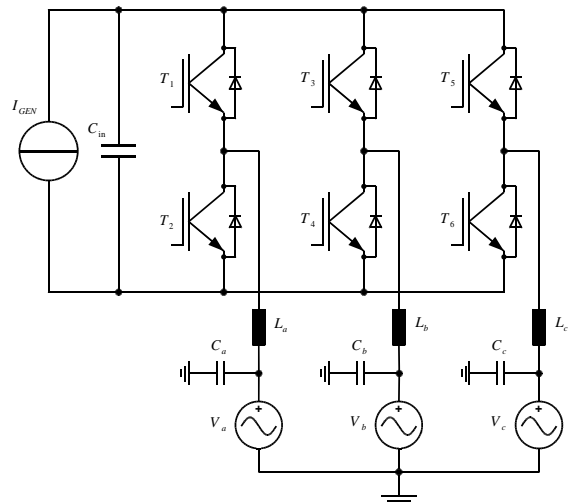


Figure 2: Analyzed three-phase B6 inverter

This topology has the following relevant characteristics:

- It is representative of medium-power inverters and it is one of the most used configurations in this power class.
- The switching strategy is capable of injecting and absorbing reactive power (if within the inverter's power specification).

4. Selected Control Strategies

Inverter control is more flexible than other machines used for power production such as synchronous or asynchronous machines. This is due to the fact that each inverter line can be controlled in a *quasi* independent manner instead of being constrained by the mechanical properties of the machine. This property gives the inverter several degrees of freedom that synchronous and asynchronous generators do not have. They can control the phase, magnitude and harmonic contents of each of

its legs voltages and thus generate a wider range of current waveforms.

It is convenient to note that this paper will focus on the most common branch of inverters: The Voltage Source Inverter (VSI), while leaving out Current Source and Z Source Inverters.

Due to the extended degrees of freedom of inverters, the FRT problem becomes especially interesting in terms of control design. The conflict of interests between power quality, grid backup, economics and inverter overloading makes the optimization process rather demanding. There are four main interests that have to be considered in FRT control design. These are presented below.

- **Power quality.** Even in fault conditions, the generators must help improving the grid quality or at least comply with the power quality requirements.
- **Grid Support.** The generator must try to help the grid in recovering from the fault. This is, in fact, in most cases the primary aim of FRT-capable generators and one of its most important priorities.
- **Economics.** The generator should try to maintain its nominal output power to prevent or at least minimize the use of choppers and lose energy. However overdimensioning requirements also impact the economic factor as they may impact the efficiency of the inverter and its initial investment. Reliability has a considerable impact in this field as well.
- **Inverter Overloading.** The overloading of the inverter should be maintained to a minimum level, although it is clear that some overloading may be necessary, it should be so that it has little or no impact on the reliability.

For the evaluation of each control strategy, the conditions presented in Figure 3 are applied. These represent a worst case scenario if the short circuit power at the point of connection is assumed to be much greater than the nominal power of the generator. Z_{fault} is chosen in such a way that the residual voltage at the Point of Connection is varied from 100% U_n down to 2% U_n .

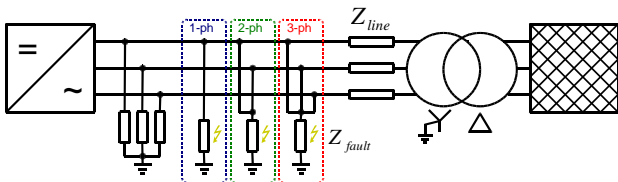


Figure 3: Assumed Fault Network with the three fault cases to be analysed.

The main purpose of this analysis is to evaluate the characteristics of the control strategies at different voltage and asymmetry levels and not the effect of each control strategy in the grid. Therefore the faults are considered at the terminals of the inverter connected to a

semi-infinite bus. Sample waveforms are presented for the normal operation and for residual voltages of 20%-21%, which is in the range of the worst case requirements of most European codes regarding FRT capabilities in Transmission networks (15-20%).

A. Synchronous Machine Emulation

The main operation principle of this strategy is to emulate the operation of a synchronous generator connected in Delta (or connected through a Wye-Delta transformer). Figure 4 shows the equivalent circuit of a synchronous machine used for fault analysis. Since the inverter has no active neutral, the ground reactance x_g'' is not present.

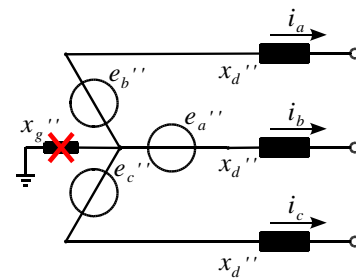


Figure 4: Pre-fault equivalent Model of a Delta-connected synchronous generator.

Since there is no neutral, the path for zero-sequence currents is of infinite impedance and thus the zero-component of the residual voltage seen by the inverter does not bring any contribution to the short-circuit current. Under this assumption any line current can be calculated as:

$$i_j = \frac{e_j'' - (U_{1,j} + U_{2,j})}{jx_d''} \quad (4)$$

Where i_j is the fault current in line j ($j = a, b, c$), e_j'' is the pre-fault EMF of line j , $U_{1,j}$ and $U_{2,j}$ are respectively the positive and negative sequence voltage phasor of line j and x_d'' is the sub-transient reactance of the machine.

Simulations were done for an inverter that emulates a delta-connected synchronous machine having a subtransient reactance of 10%¹. Figure 5, Figure 6 and Figure 7 show the current and power waveforms for the three types of faults.

It can be observed that active and reactive power fluctuations increase and can reach amplitudes of up to four times the nominal power in the case of active power and up to five times the nominal power in the case of the reactive power. The power output oscillations result from the inability of supplying zero sequence currents. Figure

¹ Typical x_d'' values are 9-17% as cited by several sources including [13].

7 shows that for symmetrical faults the fluctuations in P and Q are minimal.

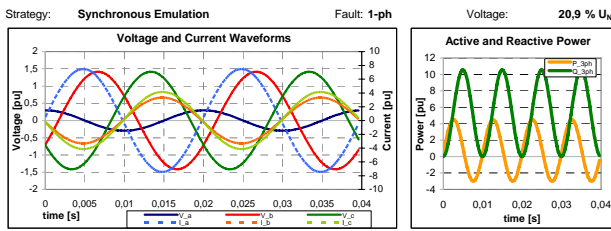


Figure 5: Waveforms for single phase-to-ground fault

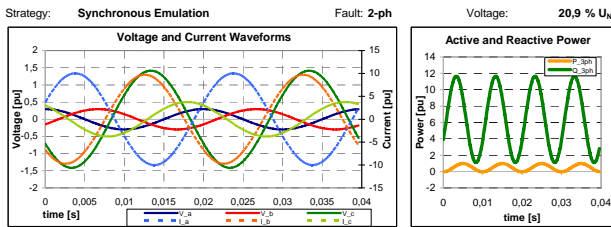


Figure 6: Waveforms for a double phase-to-ground fault

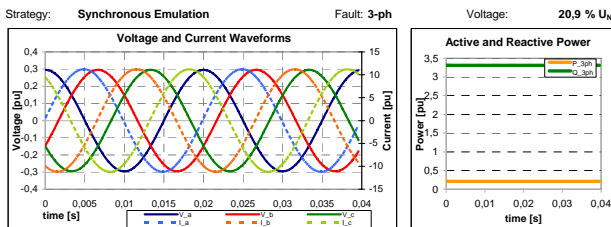


Figure 7: Waveforms for a three phase-to-ground fault

As seen in the above plots, a fault applied to this control technique produces overcurrents that could reach up to 30 times the nominal current for the proposed example. The overcurrent depends on x_d which value can be changed to reduce the overcurrent but would also impact in the grid-support capability of the converter.

Figure 8 shows the overloading characteristic of the analyzed topology. It can be seen that the factor I/I_N increases in an almost linear manner with decreasing residual voltage.

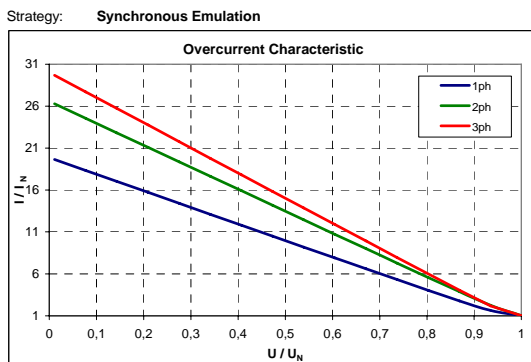


Figure 8: Overcurrent Characteristic (RMS values)

Another disadvantage of this control strategy is that depending on the type of fault, the output power may reach 10% or even less; which means that the generated power over this limit must be spilled.

Moreover, this control requires the overdimensioning of the DC-Link capacitor. Using as reference the nominal DC-Link capacitor size in the range of 0.055 pu, the overdimensioning factor can go as high as 110 (Sizes in the range of 5.5 pu). DC-Link requirements can rapidly ascend to values that are even higher than the capacitor DC-Link requirements for one phase converters.

It can be concluded that while emulating a synchronous generator is one of the most direct manner of implementing Fault-Ride-Through capabilities in an inverter, it does not exploit the full potential of inverter control and, as it has been shown, the DC-Link capacity must be enhanced. Since capacitors have a lower Mean Time To Failure than most other components, the use of more capacity may impact in the reliability of the inverter negatively.

B. Delta Instantaneous Active-Reactive Control

The Instantaneous Active-Reactive Control (IARC) has been described by [1] and is considered a valuable control strategy as it can completely control the active and reactive power injection to the grid.

This implies that the DC-Link capacitor requirements can be, at least theoretically², fulfilled with nominal DC-Link requirements. This control technique is described by [1] as follows³:

The most efficient set of currents delivering instantaneous active power P to the grid can be calculated as follows [10]:

$$i_j = gU_j \quad \text{with} \quad g = \frac{P}{|U|^2} \quad (5)$$

where $|U|$ denotes the module of the three-phase voltage vector U , and g is the instantaneous conductance that is seen from the inverter output. In this situation, the grid converter is controlled to emulate a symmetric resistance on all three phases [11]. The value of g is a constant in balanced sinusoidal conditions, but under grid faults, however, the negative-sequence component gives rise to oscillations at twice the fundamental frequency in $|U|$. Consequently, the injected currents will not keep their sinusoidal waveform, and high-order components will appear in their waveform.

As it can be seen, the method described by Rodriguez assumes that i_j may have zero-sequence components as U_j may include these components. However, the majority of three-phase inverters do not have an active neutral and thus cannot inject zero-sequence currents.

Because of this fact, a derivation of the original IARC concept was needed. This derivation was named *Delta*

² In practice, a small capacitance must be added to compensate for the reaction time and precision of the control loop.

³ Variable names have been adapted to the conventions of this document.

IARC, recalling the properties of Delta-connected generators. The resulting equations are:

$$i_j = g(U_{j,1} + U_{j,2}) \quad g = \frac{P}{|U_1 + U_2|^2} \quad (6)$$

In other words, the reference current is derived from the positive and negative sequence voltages giving only positive and negative currents.

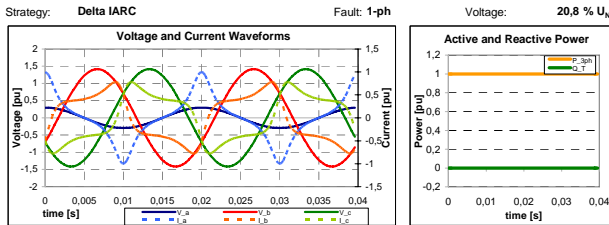


Figure 9: Waveforms at a single-phase fault condition

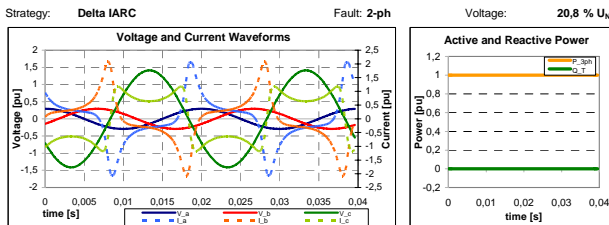


Figure 10: Waveforms during a double-phase fault

In order to maintain P and Q constant the control must inject higher order currents, which yield the distortion seen in the mentioned figures. The distortions have two main disadvantages:

1. The injection of higher currents impact negatively the Total Harmonic Distortion (THD)
2. The harmonic content changes the relation between the peak current and the RMS value of the current, which affects the loading of several components of the inverter.

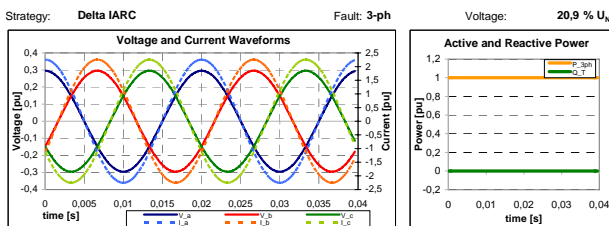


Figure 11: Waveforms during a three-phase fault

The first issue restricts from the use of this control strategy if local norms cannot be held⁴. A further analysis as to the maximal limits is being carried out but it is likely to show that one and two-phase faults (with residual voltages under 80%) are not likely to be serviced with this strategy as it is. This applies for unsymmetrical faults only as symmetrical faults will not impact the THD.

⁴ As there are no official rules for the operation during fault-events on distribution networks, current regulations (that apply only for normal operation) have been considered.

Regarding the overloading of the components, the Delta IARC provides an advantage over the simple Synchronous Machine Emulation. As it can be seen in Figure 12, the maximum overload at around 15%-20% of the nominal voltage ranges from 500%-650% of the nominal current: A value around 25% of the one required for the Synchronous Machine Emulation.

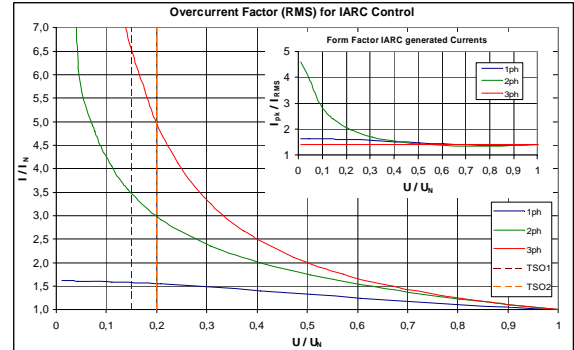


Figure 12: Current overloading using Delta IARC strategy

Nevertheless, as explained before, the form factor (I_{PK}/I_{RMS}) of the resultant current increases with decreased residual voltage. This effect implies a different loading of the different components in the inverter, especially in the instantaneous junction temperature of the transistors.

The Delta IARC strategy provides an optimal control of active and reactive power at the cost of higher harmonic contents. Up to some limits, this technique can allow injection of the full power into the grid. The peak-to-rms proportion is also one problem worth further analysis. In general, the Delta IARC Strategy may be a competitive one if it can be controlled, for example, to allow certain active and/or reactive power oscillations. A combination with other strategies that predominantly inject sinusoidal currents may be possible and could bring some of the advantages of the Delta IARC.

C. Positive-Negative Sequence Compensation

The Positive-Negative Sequence Control (PNSC) strategy is based on the premise that the active power oscillations present in an unsymmetrical system can be reduced or even eliminated if negative- sequence currents are added to the reference current. As explained by [1]⁵:

Active power P can be delivered to the grid by injecting sinusoidal positive- and negative-sequence currents at the PCC.

$$I = \frac{P}{|U_1|^2 - |U_2|^2} (U_1 - U_2) \quad (7)$$

Equation 7 indicates that the injected current and voltage vectors have different directions. Consequently, the instantaneous reactive power that is delivered to the grid is not equal to zero but exhibits second-order oscillations.

⁵ Variable names have been adapted to the conventions of this document.

In contrast to the Delta IARC Strategy, the PNSC will inject sinusoidal currents, eliminating the problem with the THD limitations but as stated by Rodriguez, this technique generates oscillations in the reactive power injection.

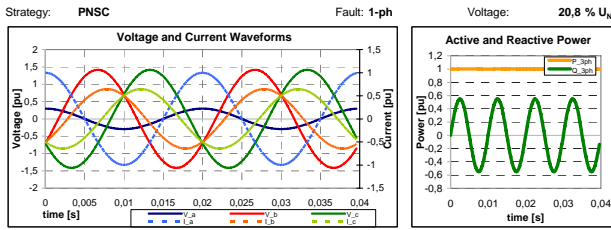


Figure 13: Waveforms for a 1-phase fault

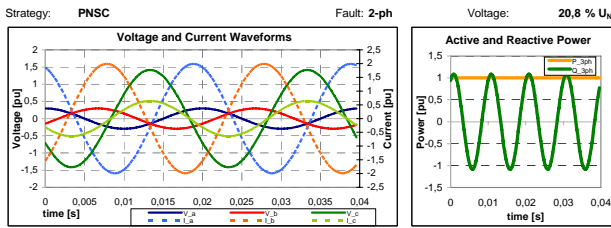


Figure 14: Waveforms during 2-phase faults

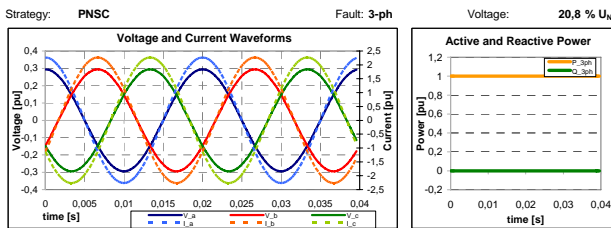


Figure 15: Waveforms during 3-phase faults

As soon as a fault is present, the PNSC will try to inject both positive and negative sequence currents so that the active power does not show power oscillations.

Nevertheless, oscillations in the reactive power are still present. It is important to note that this compensation implies an unsymmetrical reactive power distribution as well.

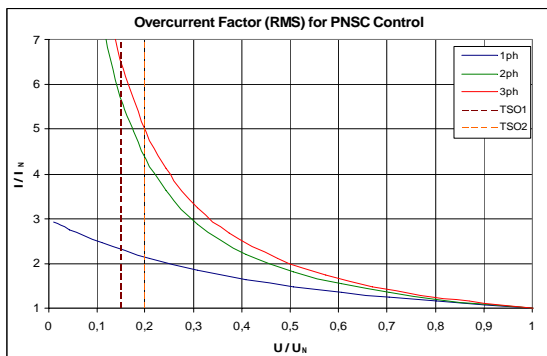


Figure 16: Overloading factor for PNSC Control

The required overload capability can be seen in Figure 16. It has a similar characteristic as the Delta IARC but has the advantage that the peak-to-rms value remains constant.

The PNSC shows promising properties such as the fact that the complete active power may be yet injected with sinusoidal currents. Nevertheless the reactive power oscillations and specially the fact that not all lines produce reactive power may not be welcomed by network operators.

5. Conclusions

The simulations performed showed that the most suitable control strategy for medium power B6 inverters to FRT is the PNSC, which shows promising properties, the IARC provides an optimal control but at the cost of higher harmonics and the less useful is the ICPS which can not exploit the the full potential of inverter control.

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