

STANDARD TEST PROTOCOL TO CHARACTERIZE ADJUSTABLE SPEED DRIVE BEHAVIOR DURING VOLTAGE DIPS

M. Teixidó¹, A. Sumper¹, Q. López¹, S. Galceran², J. Sánchez³

¹ CITCEA-Universitat Politècnica de Catalunya
Av. Diagonal, 647, 08028 Barcelona (Spain)
phone:+34 93 401 67 27, fax:+34 93 401 74 33,
e-mail: teixido@citcea.upc.es; sumper@citcea.upc.es

² Department of Electrical Engineering
E.T.S.E.I.B., UPC
Av. Diagonal, 647, 08028 Barcelona (Spain)
phone:+34 93 401 67 27, fax:+34 93 401 74 33, e-mail: Samuel.Galceran@upc.es

³ FECSA-ENDESA
Dirección de Explotación y Calidad de Suministro
Av. Paral·lel, 51, 08004 Barcelona (Spain)
phone:+34 93 509 12 32, e-mail: Jslosada@fecsa.es

Abstract.

Susceptibility of adjustable speed drives (ASD) against voltage dips it's been a red-hot issue in the last years. European standards concerning electromagnetic compatibility in the section of voltage dips don't allow characterization of ASD performance when a voltage dip occurs. Papers published about this subject are focused on the theoretical study of the effects of dips on ASD and alternative methods for testing voltage dip immunity of this equipment. But in the former, only undervoltage trip has been usually taken into account; and, in the latter, the criterion used to decide when the ASD fails is not suitable in all cases. Firstly this paper will briefly analyze why an ASD trips when there is a voltage dip. Secondly a test will be proposed with two main goals: (a) to offer a novel, simplified and affordable test protocol, and (b) to achieve test results useful for ASD users. To accomplish this second goal, energetic immunity and control immunity will be introduced to take into account process necessities where ASD is integrated.

Key words

Power Quality, Adjustable Speed Drive, Voltage Dips, Short Interruption, Voltage Dip Test

I. INTRODUCTION

ASDs are sensitive to voltage dips that occur in the power supply system. These dips are caused by short circuits, faults in transmission networks or the connection of high power loads. The consequence of this disturbance is usually the tripping of the ASD and, in some cases, results in high economical costs. Some studies have shown that voltage dips with a 20% drop during 12 cycles or more can produce a trip in the equipment [1].

There are four points which must be considered. First, the tripping of an ASD is caused by the occurrence of a voltage dip, which may even produce unbalanced voltages and phase-angle jumps. The normal function of an ASD is dependent upon the absence of voltage dips. Second, an ASD is part of a power drive system (PDS) along with the motor, auxiliary control circuits and power supply section. EMC standards fix precise operation criteria for a PDS as a whole system [2]. Thus, the system in its entirety must be considered when analyzing problems created by voltage dips as well as when defining appropriate solutions.

Third, should the effort made by ASD manufacturers to improve performance of this equipment when there is a voltage dip. Software functions to achieve higher immunity have been added in modern ASDs, like flying restart or automatic restart. However, some operations, such as automatic restart, cannot be used in all cases because they have security consequences. And fourth, it's necessary to note that in most cases, even in sensitive processes such as textile or paper, the real problem is not a temporary stop but an uncontrolled operation due to a dip. The important in these cases, it is important to control torque and speed precisely during the disturbance. Consequently, integration of an ASD in a process can improve system performance when voltage dips and short interruptions are a concern.

Furthermore, levels and techniques to realize immunity tests and performance criterion specific for PDS have been defined in European Standards [2]. A C acceptance criterion is established for PDS when affected by voltage dips or short interruptions. This means that loss of torque,

temporary degradation of performance and even system stop is allowed. Moreover, these standards also establish that realization of immunity tests isn't mandatory because of its cost.

On the contrary, users need to know ASD behavior when affected by a voltage dip. Many papers have been published in response to this necessity. These papers have focused on (a) the study and classification of these disturbances [3], (b) the analysis of its effects on an ASD [4], and (c) the proposal of test protocols to characterize ASD behavior during a dip [5], [6], [7], [8], [9]. These papers have analyzed the trip caused by the operation of undervoltage protection, but the effects of other protections, which can also produce the same result, haven't been sufficiently studied. Moreover, some proposed protocols are unaffordable due to the necessary number of tests. And finally, criteria used to decide whether ASD passes or fails is not appropriate in many industrial processes.

First, this article will discuss, why an ASD must trip when a voltage dip or short interruption occurs. Second, a standard test will be proposed with two main goals: (a) to propose a novel and affordable protocol which would reduce the number of tests necessary; and (b) to achieve test results useful to ASD users. To accomplish this second goal, energetic immunity and control immunity will be introduced to take into account process necessities where ASD is integrated.

II. VOLTAGE DIP EFFECTS ON ASD

A. Voltage dip characterization

The method most widely used to classify and characterize voltage dips is based on the different types of faults that occur in a three-phase power supply system and transformer star or delta connection [3]. This method leads to the well known classification of voltage dips into seven types; because AC drives are delta loads, dips experienced by this equipment will be reduced to types A, C, and D, shown in figure 1.

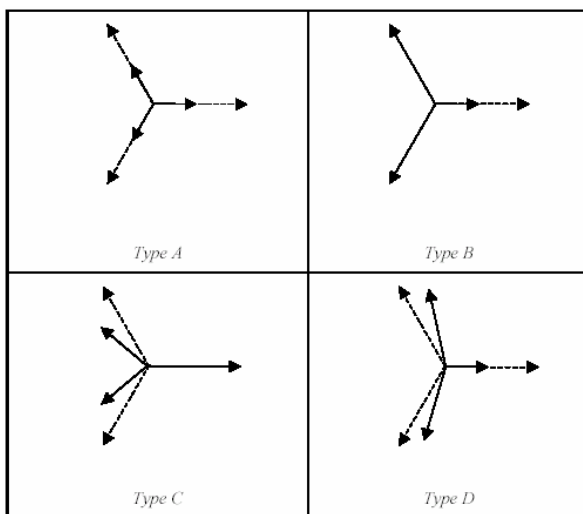


Figure 1- Classification of voltage dips

This diagram should not be confused with the usual phase diagram representing phase to neutral voltages. Each phasor in figure 1 must be interpreted as voltages measured at the equipment terminals. So in an AC drive, as a delta load without neutral, each phasor represents magnitude and argument of phase to phase voltages. This can be seen in equations (1), (2) and (3), where phase-to-phase voltages for dips type A, C and D are stated respectively. The value of V , called characteristic voltage, depends on the fault provoking the dip and the transformer connection as defined in [3].

$$\vec{V}_{ab} = \vec{V}$$

$$\vec{V}_{bc} = -\frac{\vec{V}}{2} - j\frac{\alpha\sqrt{3}}{\xi}\frac{\vec{0}}{2}\frac{\vec{0}}{\theta}\vec{V} \quad (1)$$

$$\vec{V}_{ca} = -\frac{\vec{V}}{2} + j\frac{\alpha\sqrt{3}}{\xi}\frac{\vec{0}}{2}\frac{\vec{0}}{\theta}\vec{V}$$

$$\vec{V}_{ab} = 1$$

$$\vec{V}_{bc} = -\frac{1}{2} - j\frac{\alpha\sqrt{3}}{\xi}\frac{\vec{0}}{2}\frac{\vec{0}}{\theta}\vec{V} \quad (2)$$

$$\vec{V}_{ca} = -\frac{1}{2} + j\frac{\alpha\sqrt{3}}{\xi}\frac{\vec{0}}{2}\frac{\vec{0}}{\theta}\vec{V}$$

$$\vec{V}_{ab} = \vec{V}$$

$$\vec{V}_{bc} = -\frac{\vec{V}}{2} - j\frac{\alpha\sqrt{3}}{\xi}\frac{\vec{0}}{2}\frac{\vec{0}}{\theta}\vec{V} \quad (3)$$

$$\vec{V}_{ca} = -\frac{\vec{V}}{2} + j\frac{\alpha\sqrt{3}}{\xi}\frac{\vec{0}}{2}\frac{\vec{0}}{\theta}\vec{V}$$

To define which voltage dips will be used in the proposed immunity test, worst cases will be analyzed. From (1), (2) and (3), it is clear that voltage dips with a characteristic magnitude voltage of zero are the most severe. For dips of type A, this will lead to a drop of 100%, so no voltage is applied on the equipment terminals. This is the most severe dip. For types C and D the results of a zero characteristic voltage are shown in figure 2 and 3 respectively.

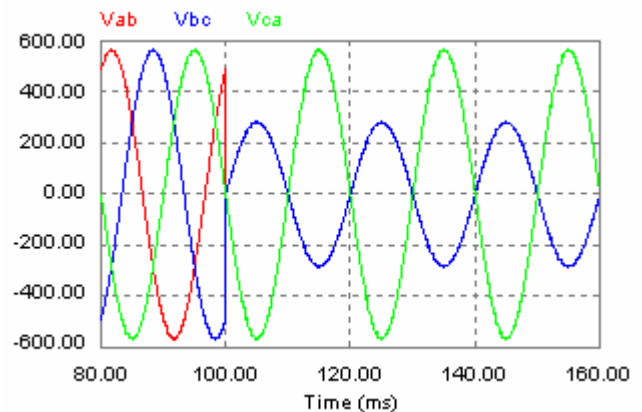


Figure 2: Type C dip phase-to-phase plot with zero characteristic voltage

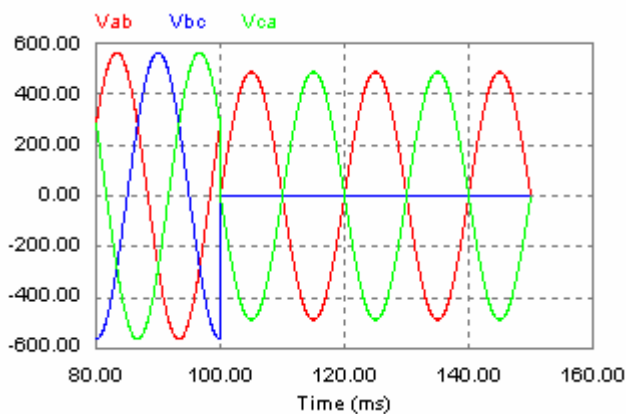


Figure 3: Type D dip phase-to-phase plot with zero characteristic voltage

It should be noted that for dips of type C there is always one phase not affected, while the other two, in this worst case, show a 50% drop and their phase angles had moved to be equal. For dips of type D the three phases are affected: one phase suffers a 100% drop while the other two have a voltage magnitude of 83%.

B. ASD must be protected against voltage dips

The performance of ASDs when a voltage dip occurs depends on the hardware, software and response time of the control. Figure 4 shows the common hardware topology used in low and medium ranges of power. This topology is known as Voltage Source Inverter.

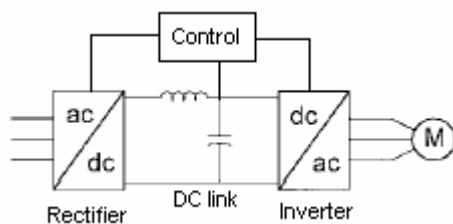


Figure 4: VSI basic topology

VSIs are indirect energy converters because they use an intermediate DC circuit to convert fixed power supply AC voltages into varying magnitude and frequency AC voltages at inverter output. This DC section allows a practical independence of the output inverter from the input rectifier. Thus, the rectifier converts AC voltage into DC voltage and its load is the DC-link. On the other side, the inverter is supplied by the DC-link and its load is the AC motor of the PDS. The capacitors in the DC-link used to reduce voltage ripple, prevent some disturbances, such as voltage unbalance or harmonics, from having an effect on the inverter operation. Even small voltage dips are resisted thanks to the energy stored in the capacitors. So energy stored in the capacitors has influence in ADS immunity, as can be seen in the next energy balance.

$$E_{\text{SUPPLY}} + E_{\text{DC-LINK}} + E_{\text{KIN}} = E_{\text{LOAD}} + E_{\text{CONTROL}} \quad (4)$$

Left-hand terms in (4) are energy suppliers and right-hand terms are energy consumers. E_{SUPPLY} is the energy

flowing from the power supply, $E_{\text{DC-LINK}}$ is the energy stored in the capacitors, and E_{KIN} is the kinetic energy of the rotating parts of the load. $E_{\text{DC-LINK}}$ and E_{KIN} values are shown in (5) and (6). On the other side, E_{LOAD} is the electrical energy consumed by the AC motor driving the PDS load, and E_{CONTROL} is the energy consumed by the control circuits of the ASD: analog, digital and communication circuits, the microcontroller or DSP, and the drivers of power switches. Although energy consumed by the AC motor is usually much higher than the energy consumed by the control, this situation changes when the ASD stops supplying the motor due to a voltage dip.

$$E_{\text{DC-LINK}} = \frac{1}{2} \cdot C \cdot V_{\text{DC-LINK}}^2 \quad (5)$$

$$E_{\text{KIN}} = \frac{1}{2} \cdot J \cdot \omega^2 \quad (6)$$

Small dips can be ridden through due to energy stored in the capacitors, however when a severe dip occurs ASD must stop its operation to prevent damages, mainly in the input side. A severe voltage dip causes a decrease in the average voltage of the DC-link. This decrease usually provokes a reduction in the AC motor speed and a loss of dynamic performance. But, if dc voltage decrease is large, sudden recovery of power supply to its rated value will cause a large current to flow into the capacitors and damage the rectifier. To prevent this, all ASD have an undervoltage protection that trips the equipment when DC-link voltage drops below a fixed level. This level varies with the manufacturer but usual values are between 70-85% of the rated DC-link voltage.

But the input rectifier can be damaged by other causes, which are often not taken into account. Figure 2 shows that in a type C dip one phase remains unaffected, so the DC-link will be charged twice per cycle. If capacitors are large enough, minimum DC-link voltage will be higher than the undervoltage level protection, so the ASD will supply the rated power to the motor. The problem is that, when the rated power is supplied, the current in the unaffected phase will increase to more than 300% and cause damage to the rectifier. A type D dip causes the same problem although rectifier currents will be lower. Consequently, an ASD must also trip when voltage unbalances appear in the supply. Protections, such as three-phase overcurrent or undervoltage, are usually integrated in ASDs to detect these dangerous unbalances.

Most papers focused on voltage dip effects on ASDs have only taken into account the operation of DC-link undervoltage protection. It is also necessary to take into account the operation of protections which detects an unbalance in the analysis the ASD behavior, and to propose some mitigation methods.

III. PROPOSAL OF IMMUNITY TEST

ASD performance in the presence of a voltage dip depends basically on:

- Type of dip: an IEC 61000-4-7 compliant dip generator has to be used to perform the dips. Moreover the generator must be able to realize type C and D dips.
- Type of load: constant horsepower or constant torque, lineal, quadratic load. This can be achieved using an AC motor fed by a FOC inverter.
- Motor speed.
- Load inertia.

1) Determination of energetic immunity curve

Energetic immunity graph will be formed by two curves that divide the magnitude-duration plane in three areas. In the outer area, the ASD will pass the dip in all cases. The inner area defines the magnitude-duration dips for which the ASD will trip always. Between these two areas the ASD may or may not pass the dip depending on the load characteristics when the dip occurs. An energetic immunity graph is shown in figure 6.

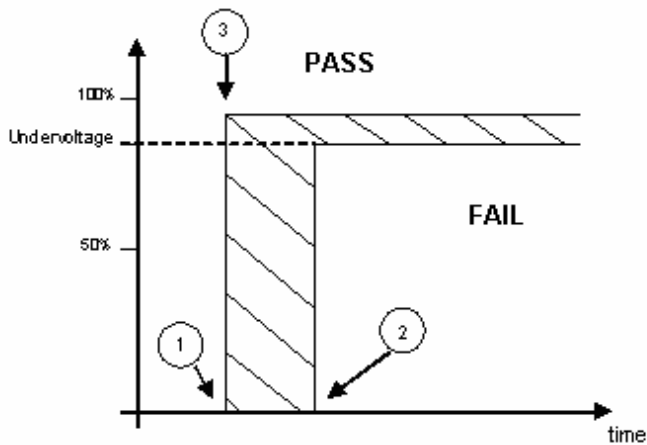


Figure 6: Voltage tolerance curve to characterize energetic immunity

In the next paragraph an optimized test will be presented. To minimize the number of tests, energetic immunity curve can be represented using the undervoltage protection level and three characteristic points determined experimentally. ASD ride-through functions must be disabled during these tests.

The point 1 of figure 6 can be obtained applying a type A dip with zero characteristic voltage when the motor is performing rated power and driving a constant horsepower load. Point 2 is obtained applying the same dip, but now motor power has to be zero, that is, motor is not loaded. Obtaining the third point may need the completion of some tests. The tripping of the ASD when power supply voltage is higher than undervoltage level protection is caused by the voltage ripples existing in the DC-link. Thus, to determine point 3, voltage dips that produce higher dc ripple will be applied, while motor is developing its rated power driving a constant horsepower load. Then, type D dips should be applied until the dip with minimum characteristic voltage that caused the ASD trip is found. However, if the ASD passes a type D dip

with a zero characteristic voltage, type A voltage dip with characteristic voltage less than 86% should be applied until obtaining the point where the ASD fails.

When these three points are determined, a voltage tolerance curve for energetic immunity can be represented as shown in figure 6. Additional tests varying type of load and inertia should be performed to confirm obtained results.

2) Determination of control immunity curve

Obtaining control immunity voltage tolerance curve will require a higher number of tests. To determine the points of the curve, ride-through functions must be enabled. The motor must produce its rated power, driving a constant horsepower load with different amounts of inertia. When the motor reaches the rated speed, type A dips should be applied with characteristic voltage ranging from zero up to undervoltage protection level, increasing the voltage 5 or 10% each time. When the supply voltage of the control circuits falls below its rated value, the points of the magnitude-duration plane can be represented.

IV. CONCLUSIONS

The behavior of ASDs when affected by a voltage dip is complicated to analyze theoretically since it depends on various parameters. Because of this, the number of papers proposing tests to characterize ASD performance has grown in the last years. But the tests proposed use a criterion to decide whether or not the ASD passes the dip, and this is not suitable in all cases. Process necessities haven't been taken into account either. The definition of energetic immunity and control immunity allows obtaining voltage tolerance curves useful to select the ASD most appropriate to the necessities of a process. Finally, the minimization of the number of tests to determine ASD immunity results in a test with minimum cost.

Acknowledgement

We would like to acknowledge the financial and technical support from ENDESA DISTRIBUCIÓN which made possible the research project on behavior of adjustable speed drives during voltage dips.

REFERENCES

- [1] H.G. Sarmiento and E. Estrada, "A voltage sag study in an industry with adjustable speed drives" *IEEE Ind. Applicat. Mag.*, vol. 2, pp 16-19, Jan/Feb. 1996
- [2] IEC 61800-3: *Adjustable speed electrical power drive systems. Part 3: EMC product standard including specific test methods.*
- [3] Math H. J. Bollen, 1999, "Understanding power quality problems. Voltage sags and interruptions" *Wiley-IEEE Press*
- [4] José Luis Durán-Gómez, Prasad N. Enjeti, Byeong Ok Woo, "Effect of Voltage sags on adjustable-speed drives: a critical evaluation and approach to improve performance" *IEEE Transac. On Ind. Applic.*, Vol. 35, No 6, Nov./Dec. 1999
- [5] Kurt Stockman, Frederik D'hulster, Kevin Verhaege, Jan Desmet, Ronnie Belmans, "Voltage dip immunity test set-up for induction motor drives" *11th International symposium on power electronics, Novi Sad, Yugoslavia, 2001*
- [6] Kurt Stockman, Frederik D'hulster, Kevin Verhaege, Marcel Didden, Ronnie Belmans, "Ride-through of adjustable speed drives during voltage dips" *Electronic Power Systems Research*, n° 66, 2003, pp. 49-58
- [7] A.K. Keus, R. Abrahams, J.M. van Coller, R.G. Koch, "Analysis of voltage dip (sag) testing results of a 15kW PWM adjustable speed drive (ASD)" *IEMDC'99*
- [8] Math H. J. Bollen, L.D. Zhang, "Analysis of voltage tolerance of AC adjustable-speed drives for three phase balanced and unbalanced sags" *IEEE Transactions on Industry Applications*, Vol.36, no.3, May/June 2000, pp.904-910.
- [9] R. Langley, A. Mansoor, E.R. Collins Jr., R.L. Morgan "Voltage sag ride-through testing of adjustable speed drives using a controllable dynamic dynamometer", 8th International Conference on Harmonics and Quality of Power ICHQP'98
- [10] SEMI F42: *Test method for semiconductor processing equipment voltage sag immunity*