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Single-Phase Single-Stage AC-DC Converter with Reduced Line-Current Harmonics

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Abstract. The circuit topology for a single-phase single stage ac-dc converter with the aim of minimising the converter's line current harmonics is presented. The circuit is based on the half-controlled ac-dc converter topology and employs active switching devices to achieve its objective. These devices are used to provide alternative paths for the line current during periods when the smoothing capacitor is supplying the load current, thus reducing the line current harmonics. Extensive simulation studies have been carried out on the circuit and results are presented and compared with the results obtained from a standard ac-dc uncontrolled converter operating under similar conditions. The results indicate that the line current harmonics are reduced to levels compliant with those set out by the relevant European Union's Directive, IEC61000-3-2, on harmonics injection into the supply mains directed at equipment that draws current $\leq 16\ A$.

Key words

AC-DC converter, minimisation of line current harmonics, IEC-61000-3-2.

1. Introduction

The number of small electrical and electronic equipment which requires low dc power for their operation**,** such as desktop computers, has been increasing at an enormous rate especially in the last decade. This dc power is typically obtained by the process of rectification of the ac mains and for small power ranges less than about 2 kW, the single-phase diode bridge ac-dc converter of Figure 1 remains the most attractive choice. This is because of its simplicity, reliability, and its low cost and low losses. The output voltage is a unidirectional pulsating waveform whose dc value is only about 63% of its peak value and thus the waveform contains large ripple voltage [1]. To reduce this ripple voltage a large smoothing capacitor is connected across the output terminals of the diode bridge. The value of the smoothing capacitor must be chosen so that the ripple voltage is reduced to, typically, 5 to 10% of the required dc voltage and it depends on the frequency of the mains, typically 50 Hz, and on the value of the load current. The smoothing process whilst increasing the dc value of the output voltage waveform has an adverse affect on the supply current drawn by the converter. The smoothing capacitor causes the line current to flow only for short intervals of time as shown in figure 1(b).

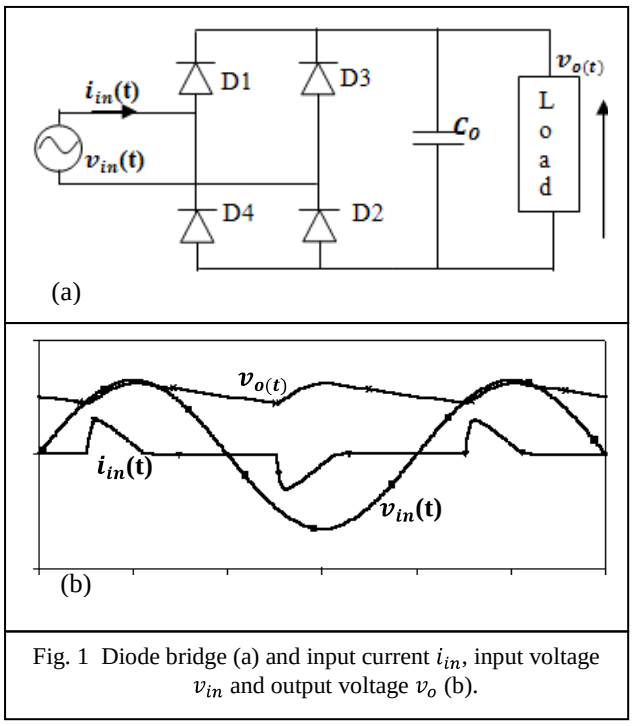

Fig. 1 Diode bridge (a) and input current i_{in}, input voltage v_{in} and output voltage v_o (b).

For the remaining time the capacitor supplies the load current. That is the supply current consists of short narrow pulses. This means that the input current is rich in harmonics. The generated harmonics will be injected into the supply mains and may be harmful to other equipment connected to the mains. Further, if there is a

large number of such converters connected to the mains, the mains conductors have to be over rated to allow for these current harmonics.

In order to limit the generation and injection of such unwanted harmonics, national and international regulatory bodies, such as the International Electrotechnical Commission (IEC), have the task of setting standards that regulate the generation and injection of harmonics. The harmonic standard IEC-61000-3-2 sets the limits for Class D electrical equipment [2]**.** This class refers to equipment that draws an input current up to a maximum of $16\ A$. The converter presented here falls into this category. The IEC limits for class D equipment are presented in Table 1.

Table 1: IEC61000-3-2 standard for class D equipment.	
Class D: Single-phase, under 600 W, personal computers, PC monitors, TV receivers.	
Harmonics (n)	Class D (mA/W)
3	3.4
5	1.9
7	1.0
9	0.5
11	0.35
13	3.85/13
$15 \le n \le 39$	3.85/n

These limits have been continuously tightened over the years. For example, the limit for the third harmonic current for power levels up to 600 W is 3.4 mA/W compared to 2.3 A/W in the older IEC-555 standard which became obsolete in 1995. These new standards have placed onerous demands on the design of ac-dc converters with reduced harmonic currents that meet the IEC regulations. In pursuing this objective, various circuit topologies have been described in the literature. One of the most popular topologies is shown in Figure 2. This utilises a PWM dc-dc boost converter which reduces the line current harmonics and improves the input power factor.

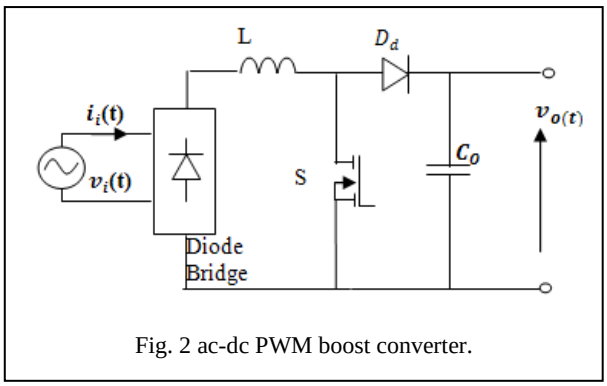

Fig. 2 ac-dc PWM boost converter.

A number of dedicated integrated circuits such as the FAN6982 exist that implement PWM dc-dc boost converter [3].

Although, good power factor correction and harmonic reduction can be achieved with the above boost topology, the circuit has some drawbacks. It is a two-stage converter which complicates the circuit and reduces its reliability and there are three semiconductor devices in series in the path of the power flow. In addition, the high switching frequency of the boost converter increases the power loss which reduces the efficiency and reliability of the converter. Several alternative single-stage ac-dc converter topologies with varying degrees of complexity and performance have been proposed in the literature [4], [5].

2. Proposed circuit and its operation

The proposed circuit is shown in Figure 3. It is a half-controlled bridge ac-dc converter employing two MOSFETs as switches. The circuit has the advantages that at any instant there are only two semiconductor device volt drops in series with load, the drive voltages for the MOSFETS are referenced to the same earth, and there is no need for a dc side inductor. Further, the switching frequency is lower than that required for the boost circuit which reduces the switching losses.

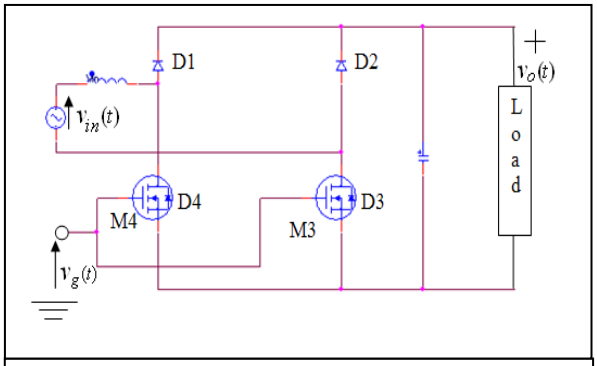

Fig. 3: Half-controlled AC-DC converter.

The operation of the circuit may be divided into four modes of operation and is explained with the aid of the diagrams in Figures 3 and 4.

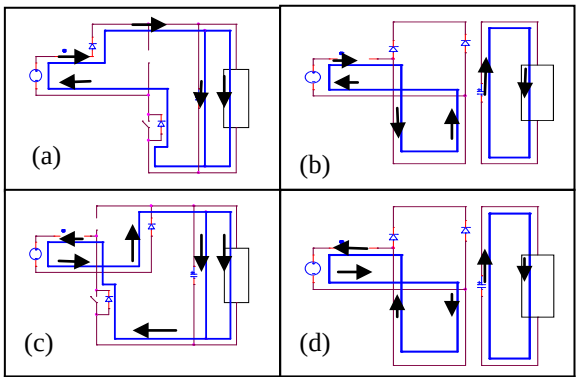

Fig. 4: Modes of operation of the circuit.

Mode 1

In this mode the supply voltage is positive and the switches M3 and M4 are open. As shown in Figure 4(a), the supply current flows through D1, the load and the capacitor and back through the integral diode of M3.

Mode 2

The input ac voltage is positive and the transistor switches M3 and M4 are turned on. In this case, Figure 4(b), the supply current flows through M4 and back through the integral diode of M3. The load current is supplied by the capacitor.

Mode 3

This mode is illustrated in Figure 4(c). The supply voltage is negative and the switches M3 and M4 are open. Current flows out of the source through D2 and through the load and the capacitor and back through the antiparallel diode of M4.

Mode 4

In mode 4, Figure 4(d), the supply voltage is negative and the switches M3 and M4 are closed. The capacitor discharges and furnishes the load current, whilst the supply current is returning through the switches M3, and the antiparallel diode of M4 and the input inductor.

3. Results

AD-DC converters with power ratings of 340 W, 240 W and 180 W were designed using both converter topologies i.e. the uncontrolled diode bridge circuit of Figure 1(a) and the half-controlled bridge of Figure 3. For each circuit and each power rating the design parameters e.g. ripple voltage, are the same for the both versions of the converter topologies.

3.1. The Uncontrolled Converter

Table 2 shows the line current harmonic density in mA per watt (mA/W) of the dc output power. The Table also shows the relevant IEC61000 limits.

Table 2: The mA/W line current harmonic in the uncontrolled converter for various dc output powers.

Harmonic order (n)	DC output power (W)			IEC Limit
	340 W	240 W	180 W	
	mA/W	mA/W	mA/W	mA/W
3	15.76	15.48	14.11	3.400
5	8.24	9.29	9.11	1.900
7	2.74	3.85	4.34	1.000
9	1.54	1.48	1.51	0.500
11	1.24	1.40	0.13	0.350
13	0.65	0.85	0.97	0.296
15	0.62	0.58	0.54	0.257
17	0.42	0.54	0.50	0.226
19	0.35	0.35	0.40	0.203
21	0.30	0.32	0.28	0.183

It is evident that for all current harmonics the mA/W harmonic densities are well above the levels specified by the IEC61000-3-2 standard, rendering the basic diode bridge ac-dc converter, as it stands, impractical.

3.2. The Half-controlled Converter

A simple switching strategy was used to generate the gate PWM drive signal for the two MOSFETs in the Half-controlled circuit of Figure 3. The objective was to increase the conduction time of the supply current and hence minimise its harmonic content. As shown in Figure 5(a), this PWM signal is generated by comparing a full-wave rectified sinusoidal signal, sampled from the secondary of the converter's multi-tapped input transformer , to a 10 kHz triangular waveform. The PWM drive signal is shown in Figure 5(b). Table 3 shows the line current harmonic densities (mA/W) for various values of dc output power. It is clear that the harmonic currents are within the levels set out by the IEC61000 standard. Further, as can be seen from Figure 6, the line current waveform is near-sinusoidal.

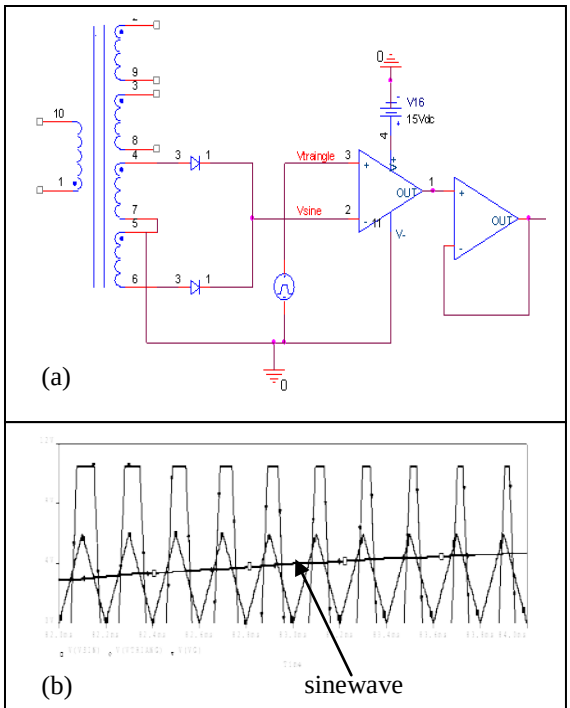

Fig. 5: (a) Circuit for generating the MOSFET drive signal and (b) the waveforms.

Table 3: The mA/W line current harmonic in the half-controlled converter for various dc output powers.

Harmonic order (n)	DC output power (W)			IEC limits
	340 W	240 W	180 W	
	mA/W	mA/W	mA/W	mA/W
3	2.765	2.917	3.017	3.400
5	0.588	0.771	0.817	1.900
7	0.462	0.583	0.672	1.000
9	0.335	0.442	0.500	0.500
11	0.268	0.367	0.444	0.350
13	0.206	0.304	0.372	0.296
15	0.179	0.246	0.311	0.257
17	0.147	0.200	0.472	0.226
19	0.106	0.158	0.167	0.203
21	0.082	0.092	0.167	0.183
23	0.062	0.092	0.122	0.167
25	0.041	0.067	0.094	0.154

4. Conclusions

A simple circuit topology, of a half-controlled full-wave bridge ac-dc converter, with the objective of reducing its line current harmonics was presented. The circuit was tested with power levels of 340 W, 240 W and 180 W, and in each case the line current harmonics, up to

harmonic order n=39, were investigated and found to be compliant with the EU directive IEC61000-3-2.

References

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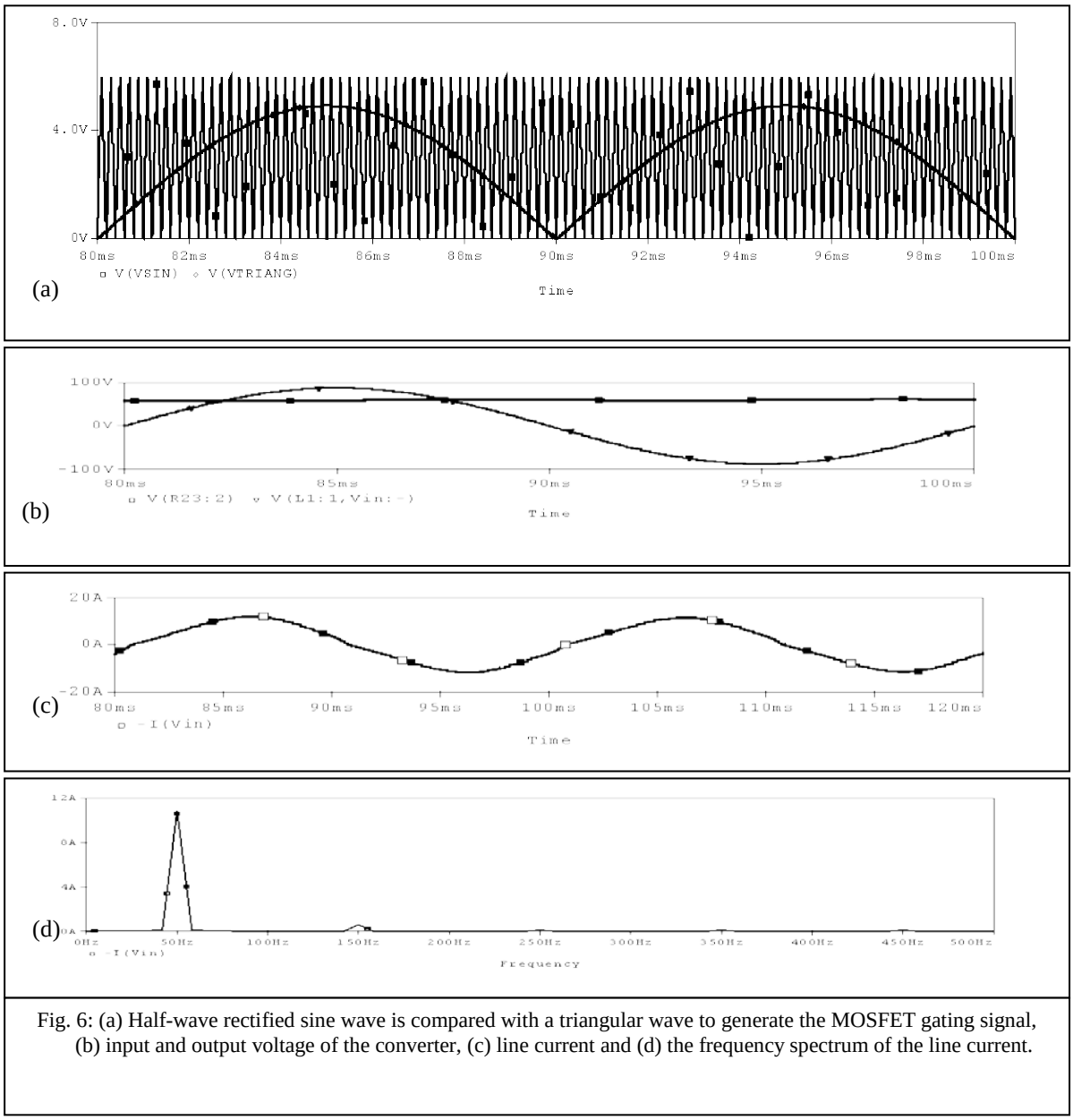

Fig. 6: (a) Half-wave rectified sine wave is compared with a triangular wave to generate the MOSFET gating signal, (b) input and output voltage of the converter, (c) line current and (d) the frequency spectrum of the line current.