

Reduced Losses in PV Converters by Modulation of the DC Link Voltage

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Abstract. The efficiency of a PV system has improved by the fact that the researchers have used different techniques to enhance their efficiency. This paper aims to present how the PV converter losses can be reduced by employing a polypropylene capacitor in the DC link and to modulate that DC voltage. A problem of controllability and stability arises. Two current control methods, constant off time and a PWM type with second order high pass filter DC-link feedback are presented. Polypropylene capacitors in the PV converters do have lower losses and a lower cost. The PV converter simulation and lab experiment is based on a three-phase bridge APTGF50X60T3G, used to combine a step-up/step down and H-bridge in one package.

Key Words

DC link voltage, polypropylene film capacitors, constant off time peak current control, PWM high pass filter feedback, cost effective PV converter.

1. Introduction

Many manufacturers from all over the world made the PV modules affordable as a lot of investments research and development have been done to achieve this. However, the total cost of a PV system includes also the cost of the inverter and the cost of installing. The grid connection cost, and installation cost still remained rather high [4], and are depending on the local labor cost. For the PV converters, still some cost optimisation could be done. One can consider a change in the choice of components, topology and control to try to achieve this. Many inverter technologies have been using the electrolytic capacitors in the DC link since their cost/ μF was affordable compared to other capacitor types. However, due to their technology, the electrolytic capacitors have a low ripple current rating [1]. For this reason, in order to reduce losses in the PV inverter technology, some companies have started to use the polypropylene film capacitors. Nevertheless, the use of these capacitors requires a good study so that they can be cost effective [1]. The use of a standard three-phase module for single phase injection [Fig.1] could give new opportunities in easy assembly.

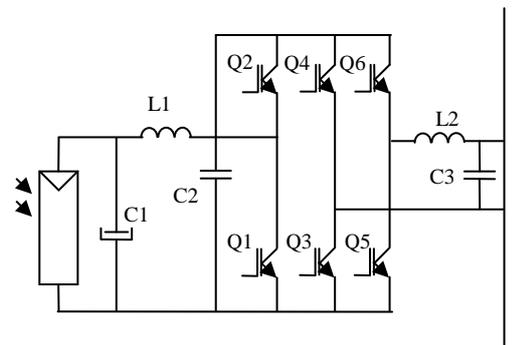


Fig.1 Single phase PV converter using a three-phase bridge

In the mean time, a configuration with a small polypropylene DC-link is tried out. Fig.1 presents a converter topology that uses a three-phase bridge, but it uses it in a different way for single-phase injection. The topology is some kind of LCL filter, with a boost or buck conversion action in between. The use and advantages of the LCL filter have been described in [5],[6] and [7]. The advantage in this case is a lower current ripple at both input and output. The capacitor C1 is used here at a typical 150-250 V and is much larger in value and size than C2. Fig 2 shows that the voltage on capacitor C2 is constant when the instantaneous grid voltage is low. Q3, Q4, Q5, and Q6 make a single phase H-bridge where C3 and L2, make a low pass filter for EMC. In the H-bridge, Q3 and Q4 are switched depending on the quadrant whereas Q5 and Q6 are switched depending on the quadrant and PWM modulated. This allows using only one low pass inductor in the output. Fig. 2 shows the waveform on C2. In a transistor module, the outer legs are better cooled than the mid-leg and can afford a bit higher losses due to switching.

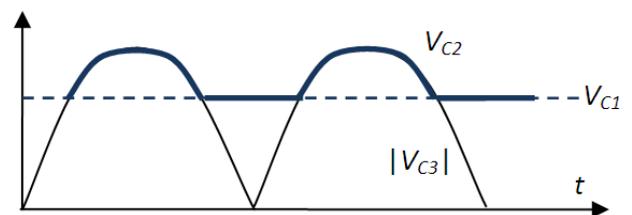


Fig.2 Control voltage across C2 capacitor

The topology offers several advantages. The switching loss in Q1 is limited as the voltage across the C2 is lower than usual, and it switches only a part of the time. The capacitor C2 is a low loss type and the capacitor C1 is large and helpful to reduce EMC (Electromagnetic Compatibility). The switching losses in Q5 and Q6 are limited since on the top of the sine they do not switch.

The slow leg Q3-Q4 permits to use only one active filter inductor L2 to lower the EMI (radio interference) from PV to grid. However, the topology does also show some disadvantages. The control of the convertor is not obvious, as one faces a 4th order circuit or even more when the grid impedance is considered. The reason of the difficulty is that C2 is a foil capacitance with low capacitance value.

The inductors L1 and L2 play a big role in the PV converter. The direct hard switching with high di/dt at the output level of the PV converter is reduced because of the presence of the inductors, and as switching occurs at a typically lower voltage. This makes the conversion smoother and with less EMC problems. Also the losses in C2 are very low compared to electrolytic capacitors. However, the question remains if the convertor is stable enough and if it can be controlled well. This will be investigated in this paper.

Fig.3 shows the current mode control of the PV converter. The voltage at the output of the bridge is used to control the current in L2. The current control for the topology makes the system work in four quadrants. The way of control results in some kind of multilevel action without being a multilevel converter topology.

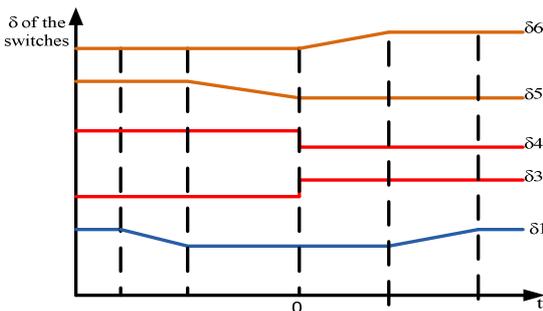


Fig.3 The PV converter switches behavior
x-axis: desired voltage at the output of the H-bridge
y- axis: the duty ratio of the switches to be operated.

2. Losses in a PV Converter Link

2.1 Module Conduction Losses

Losses in a PV converter can be originated from different sources. One non-negligible source is from the switching of the power electronic devices [2]. Since the switching is at high rate of current, the DC link bus must have a low ESR capacitor in order to reduce the losses. If a

polypropylene film capacitor is used, the ripple current is less limiting. Instead, the voltage ripple is important, but this is not a big problem in the DC-link. The switching loss calculation in PV converter [Fig.1] is based on the APTGF50X60T3G module data sheet and on the dc link voltage modulation [Fig.2]. However, the following equations are used to evaluate the conduction losses in the PV converter [2].

$$P_{CV,Q} = \frac{V_{CE,O} \hat{I}_L}{2 \cdot \pi} \int_0^\pi \sin(\omega t) \cdot \frac{1+M(t)}{2} + \frac{r_{CE,O} \hat{I}_L^2}{2 \cdot \pi} \int_0^\pi \sin^2(\omega t) \cdot \frac{1+M(t)}{2} \quad (1)$$

$$P_{CV,D} = \frac{V_{F,D} \hat{I}_L}{2 \cdot \pi} \int_0^\pi \sin(\omega t) \cdot \frac{1-M(t)}{2} + \frac{r_{F,D} \hat{I}_L^2}{2 \cdot \pi} \int_0^\pi \sin^2(\omega t) \cdot \frac{1-M(t)}{2} \quad (2)$$

$$P_{CV} = 6 (P_{CV,Q} + P_{CV,D}) \quad (3)$$

Where ω is the current's angular frequency, $V_{CE,O}$ is the IGBT's threshold voltage, r_{CE} is the IGBT's differential resistance, $V_{F,O}$ is the diode's threshold voltage, V_f is the diode's differential resistance and $M(t)$ is the modulation function, $P_{CV,Q}$ and $P_{CV,D}$ are conduction losses in IGBT and in diode respectively.

In the considered module, the transistor voltage drop is very close to the diode voltage drop. For the H-bridge, the eq.2 and eq.3 show that, using a lower DC-link voltage increase $M(t)$. In the boost converter, the diode losses increase and the transistor losses decrease by almost the same amount. So, for the total module, the DC link modulation has almost no effect on the losses.

2.2 Switching Loss Calculation

In most of topologies, the switching losses are not negligible compared to the conduction losses.

The switching loss can be estimated in [eq.4].

$$P_{sw} = f_{sw} \cdot \left(\int_{t_1}^{t_1+t_{swon}} i_s \cdot V_s dt + \int_{t_2}^{t_2+t_{swoff}} i_s \cdot V_s dt \right) \quad (4)$$

Where f_{sw} is the switching frequency, i_s and v_s are respectively instantaneous current and voltage through the IGBT, t_1 is the IGBT ON starting time, t_2 is IGBT OFF starting time, t_{swon} is the IGBT ON time and t_{swoff} is the IGBT OFF time. One can see that the losses are rather proportional to the frequency and voltage. E_{on} and E_{off} are given by the manufacturer [3]. Some overall optimizing result was done by considering the switching

frequency of 25 kHz. However the optimum choice is quite flat. The frequency is a tradeoff between switching losses, EMI and inductor losses.

2.3 Losses in the DC link capacitors

The DC link losses in C2 are mainly depending on the high frequency current in C2, It is in the order of 10A rms for the considered power. Typical electrolytic capacitors may have an ESR at 10 kHz of about 50 mΩ in hot condition, and cold significantly more. A polypropylene capacitor such as MKP1848S has an ESR of 17mΩ, two in parallel 8.5 mΩ. Also the price is about 10 times lower. In the proposed converter, the losses in C1 are mainly 100Hz losses, these losses still are present due to the fact that the power to the grid pulsates with 100Hz in the grid. The high frequency current ripple in C1 is low. Moreover one can oversize C1 without start-up problems as the capacitor is charged by the PV and not by the freewheel diodes of the H-bridge and the grid. The ripple on C1 is used afterwards for MPPT (Maximum Power Point Tracker).

3. Constant off Time Peak Current Control

3.1 Principle

Current mode control at constant frequency is well known but it has a risk of instability at half of the switching frequency. If the frequency is not kept constant, several variants are known [8]. Here, the “constant off time peak current control” (COPCC) is chosen since it has the advantage to include protection in the same item as the control. It switches off when the set current is reached and then a fixed off time is applied. In contrast, the COPCC is stable for all duty ratios [Fig.4], but it does not keep the frequency constant. This type of control is often used in LED converters and is also good in motor control [9]. Fig. 4 shows the principle of the COPCC. Note that the duty ratio is beyond 50% are obtained without any stability problem.

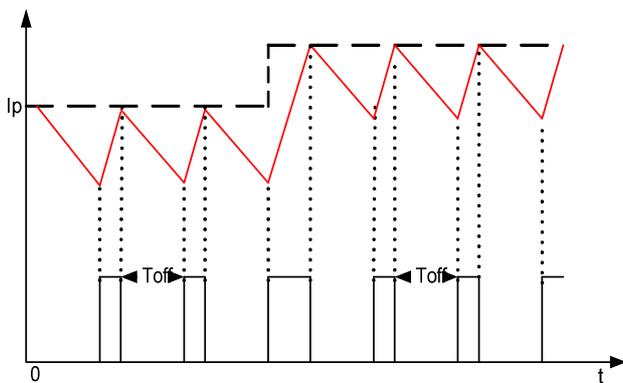


Fig. 4. Constant off Time Peak Current Control

3.2 Simulation

Fig.5 presents the principle circuit of the COPCC. The NO switch closes while the input goes high. The elements in circuit were calculated in order to get 25 μs as off time. It acts like a retriggerable monostable multivibrator.

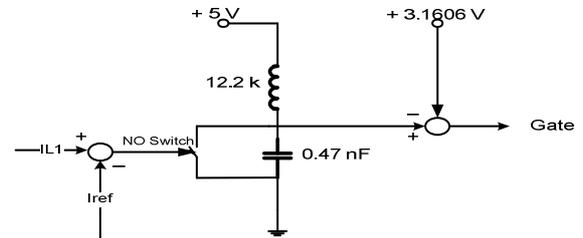


Fig.5. Constant off Time Peak Current Control Circuit

Fig.6 presents the principle circuit of constant off time peak current control with high pass filter feedback on the voltage of C2, to damp resonances on C2. The idea is that the high pass filter compensates for the phase delay at the resonance frequency. In this way, one can actively damp the resonance. In the case of the COPCC, the averaged phase delay is some half period of the frequency for this type of control.

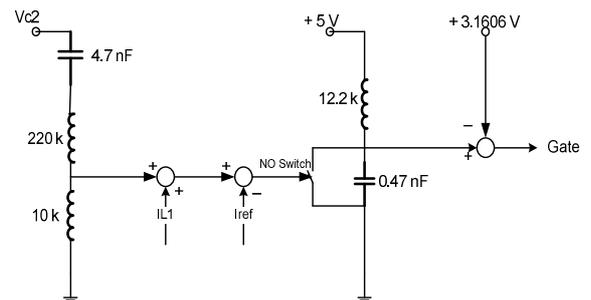


Fig.6. Constant off Time Peak Current Control Circuit with high pass filter feedback

The simulation was performed based on the values of Table I. The simulation goal is to test the dynamic of the DC link of the PV converter topology using the naked COPCC [Fig.5] and the COPCC with high pass filter feedback [Fig.6]. Adding a high pass filter feedback [Fig.6] into the constant off time current control, improves the stability of the system [Fig.8] and [Fig.9]. The input voltage is 100 V and the output voltage is 200 V. The current reference as voltage image is 6 Amps with superimposed square wave of 1 Amp amplitude, and a frequency of 125 Hz. Fig.7 shows the response. Moreover, it shows that there is some resonant frequency. However, constant off time peak current control with HPF feedback stabilizes the system [Fig.8]. The system gets well damped and has a reasonably fast step response. To simulate the low impedance of the grid, an electrolytic capacitor was put at the output.

Table I. Converter materials

Material	Type	Value
Capacitor, C1	electrolytic	2200 μ F
Capacitor, C2	Polypropylene film	20 μ F
Capacitor, C3	Polypropylene film electrolytic	2200 μ F
Inductor, L1	Amorphous iron	500 μ H
Inductor, L2	Amorphous iron	1400 μ H
IGBT	APTGF50X60T3G	-
DC source V1		100V
Load	Resistive	50 Ω

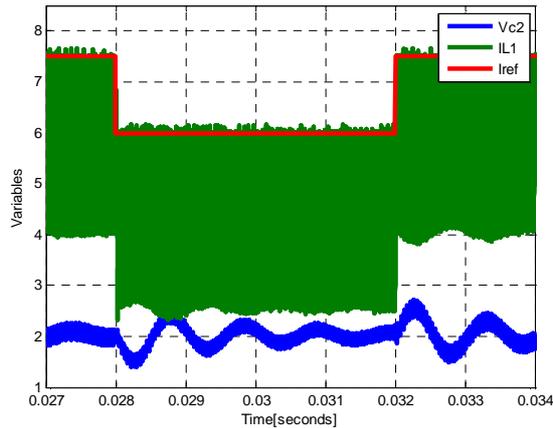


Fig. 7. Current in L1 and DC-link voltage using Constant Off time Peak Current Control without feedback

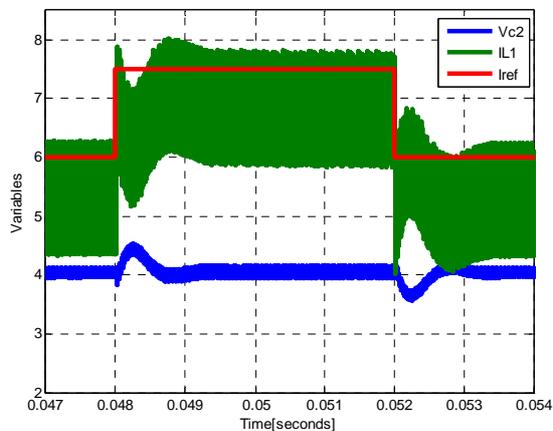


Fig.8. Current in L1 and DC-link voltage using Constant Off time peak current control with HPF feedback.

3.3 Lab Experiment

The step up is mainly composed of the power stage (top side), the constant off time current control (middle part), and the over voltage protection (bottom part) [Fig.9]. The conducted experience is based on the simulation presented in the previous section. In the step up mode, the system is stable without feedback, whereas in the step down mode, the system is even unstable in open loop. The analyses of the system are made by referring on the simulation and lab experiments results. In [Fig.10] and [Fig.11], the channel 2 is the current, the purple

channel is reference current and yellow channel is the voltage. The lab results and the simulation show a similar dynamics of the system. Fig.10 and Fig.11 show that the output voltage is 178 Volts. This is due to the fact that the input voltage was 89 Volts. However, the response in Fig.7 has the same dynamic behavior as the response in Fig.10. Similarly, the response in Fig.8 and Fig.11 are quite the same.

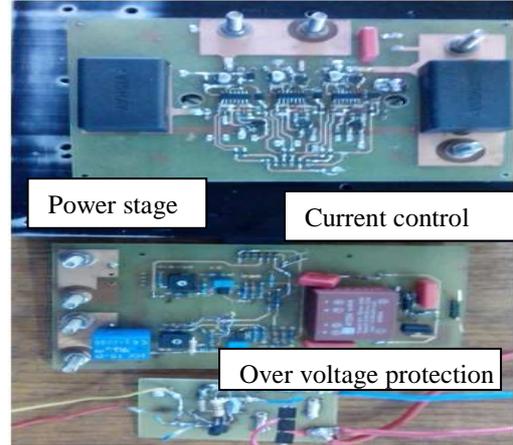


Fig. 9. Buck-Boost Converter Step Up

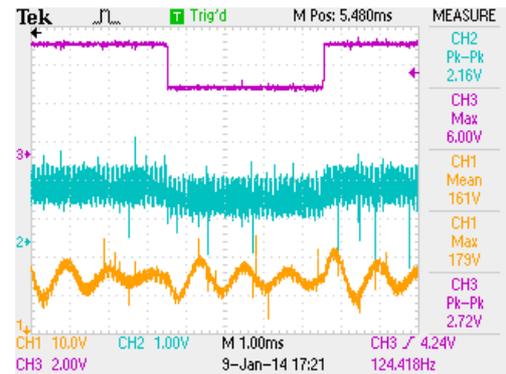


Fig. 10. Constant Off time Peak Current Control without HP feedback

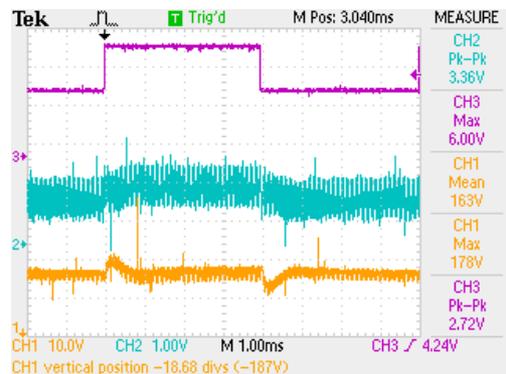


Fig.11. Constant Off time peak current control with HP feedback.

Constant off time peak current is fast but it is not easy to implement it using microcontroller in order to operate in four quadrants [Fig.3]. For this reason, the paper presents another technique, PWM high pass filter feedback, which can be more powerful than the previously discussed

method. It is not discussed here, but one can show that the control of a step down converter in current mode control is unstable due to L1 and the small C2. In experiments, the circuit goes in overvoltage protection.

4. PWM High Pass Filter Feedback

4.1 PWM Simulation build up

Digital circuits are quite convenient for power electronics [8]. Some digital circuit limitations, PWM resolution and so on, are not any more a challenge because with a good design and selection of microcontrollers, it is possible to overcome it. The current control described in this paper is based on the control of the duty ratio of the boost and buck boost converter [Fig.12]. While damping the resonance in C2 one can do more: digitally, it is possible to control IL2 directly while one is controlling δ_1 where the peak current control is controlling only IL1, and it would still need further control operations such as feed forward. The main drawback of digital control is that one introduces a delay due to sampling, conversion to digital, calculating and applying it to compare with a saw tooth.

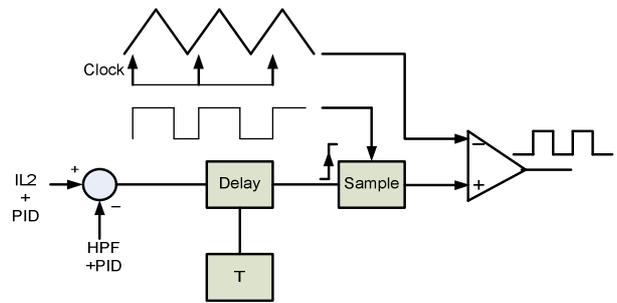


Fig.12 Sampled PWM Block Diagram IL2

Typically there is about one period delay in the control of a duty ratio, and even more in current control. A low pass LCL circuit has typically almost no phase shift at low frequency and 180° phase lag at high frequency. So, to damp the resonance, a 90° phase lead should be given. And also some phase advance to compensate for the delay of the processor based PWM. To obtain that one needs a second order high pass filter. On one hand it is not so obvious to implement it digitally as the calculation of second order high pass filters needs several samples and also time. On the other hand it is difficult to absorb it in a PID controller.

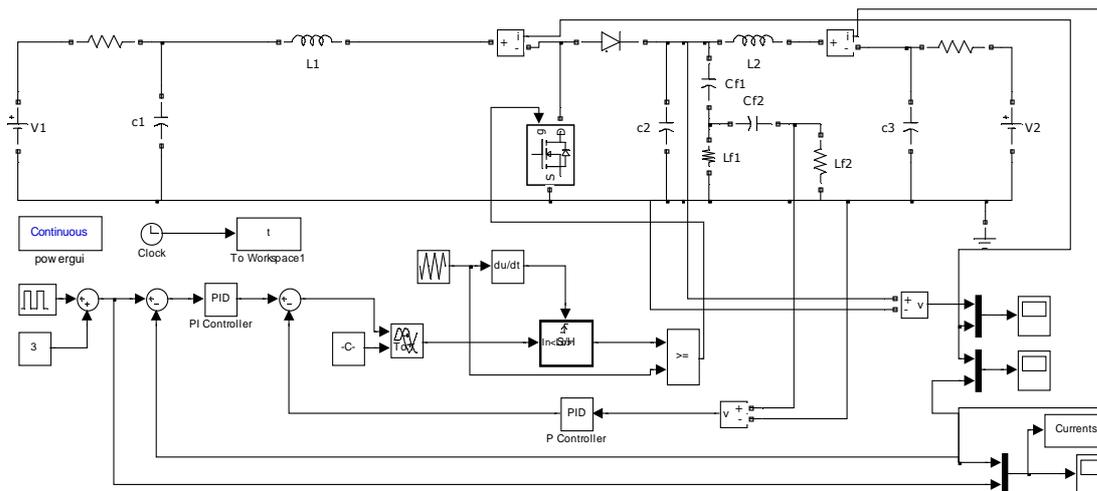


Fig.13. The PV converter current mode control block diagram

Normally, one expects that the DC link voltage must be measured. However, the second order HPF of the DC link voltage is sampled instead of sampling the DC link voltage. This saves time. The second order also limits the amount of ripple on the measured signal, compared to a pure differentiating action.

4.2 PWM High Pass Filter Feedback Simulation

Table I shows the values that were used to test the DC link of the PV converter. Both step up and step down are tested. Fig.13 presents the circuit diagram of the converter. The C2 value was changed from $20 \mu\text{F}$ to $10 \mu\text{F}$ in order to tune easily the control. The high pass filter damps all resonant frequencies from the DC link. The grid is modeled as back EMF.

Now that, the PV converter hosts three parts: Step up DC converter and step down DC converter, and H-bridge, it is necessary to test each part separately.

Therefore, the step up converter is first simulated and secondly the step down is simulated as well. Fig.13 shows the boost converter current-mode control using the second order high pass filter. The time constants are $30 \mu\text{s}$ and $60 \mu\text{s}$ for the first and second high pass filter, respectively. On one hand, the PID current control has only one component, integrator. On the other hand, the second order high pass filter PID is proportional active controller. The results of the controller are found in Fig.14 and Fig.15. From Fig.14, It is obvious that the step response of the system is stable. It is even fast if one considers the parasitic resonance of C2. The reference current is a step function [Fig.14].

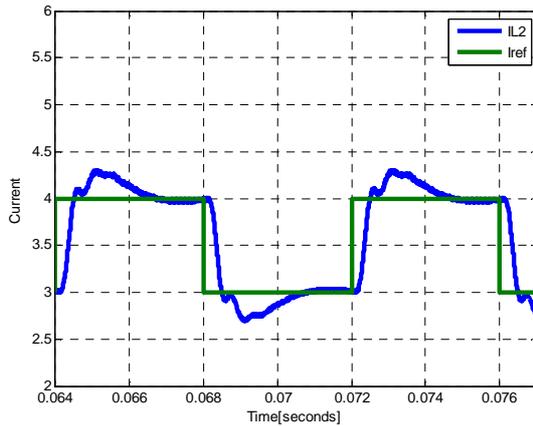


Fig.14. Iref and **IL2** while controlling the Boost converter

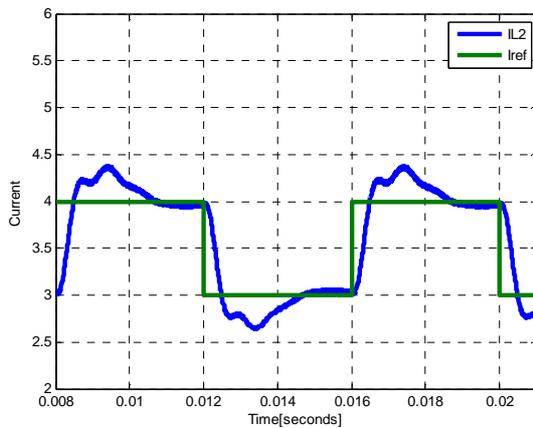


Fig.15. Iref and **IL2** while controlling the Step down converter

In another part of the period, to control the same current **IL2** using $\delta 2$ was as well successfully simulated with the same PI controller [Fig.15]. All in all, the simulation tests of both converters (step up and step down) reveal that the control of the H-bridge can be easily achieved. In other words, it is obvious that the whole system can work as long as the DC link voltage is well controlled. It must be emphasized that the current in L2 can be controlled using the same high pass filter feedback for the damping, for both boost and H bridge operation, although different transistors are controlled. However, between both modes of Fig. 14 and 15, the gain of the PI and P controller have to be adapted.

5. Future Work

Up to now we show that the control of both buck and boost part can be stabilized and that The current in the inductor L2 can be controlled. The future work will be to implement, the control of the four quadrants of the inverter by employing the PWM high pass filter feedback control according to [Fig.3].

6. Conclusions

For single phase grid injection, a three-phase bridge topology can be used while using the left leg as a boost converter and with reduced, film type DC-link capacitor. However, the behavior tends to have a pronounced resonance for the step-up converter; for the H-bridge it is even unstable. One hand, this pronounced resonance can be damped using an analog constant off time peak current control using a first order high frequency filter to stabilize the resonant frequency. On the other hand it can be controlled by a fast duty control in a digital processor, while sampling a second order high pass filter. At low instantaneous grid voltage, the H-bridge is modulated, When the grid voltage is higher than the DC input voltage, the current to the grid can still be controlled with the step up converter without switching in the H-bridge. The controllability of the current reduces the switching losses of the PV inverter.

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