Modeling, Simulation and Reduction Techniques of Electromagnetic Conducted Emission Due to Operation of Power Electronic Converters

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Abstract. High frequency and high speed switching in power electronic circuits causes electromagnetic interference. One of the problems that electronic and electrical engineers are faced with is to present their designs of power electronics circuits in compliance with electromagnetic compatibility regulations. In this paper some operative software and hardware methods to mitigate the conducted electromagnetic interference due to the operation of power electronic circuits are introduced. The effectiveness of these interference suppression techniques are investigated by simulation of some common PE circuits using appropriate software. The simulations are conducted with and without considering the mitigation techniques. Simulation results show improvement in performance of power electronic converters in point of view of electromagnetic compatibility.

Key Words

Converters, Electromagnetic Compatibility (EMC), Electromagnetic Interference (EMI), Mitigation techniques, Power electronics

1. Introduction

The increase of switching speed and frequency in power electronics converters has greatly improved their performances and characteristics [1]. These advantages are accompanied with the increased level of interference, so that EMI consideration is a major task for circuit designers nowadays [2]. In order to limit of interference, national and international regulations have been established where compliance with these regulations in European and developed countries is mandatory [3].
Investigations show that not only the level of EMI due to power electronics converters is not in compliance with regulations but also in some cases no consistency is observed [4]. It is clear that countermeasures are required in order to mitigate the level of interference. Several strategies to suppress electromagnetic interference have been proposed in the literature [5]. In this paper some operative conducted EMI mitigation techniques are discussed. Mitigation techniques are classified in two groups. The first group includes filtering, snubbing, grounding and Printed Circuit Board (PCB) or layout considerations. In the second group, effects of switching characteristics such as frequency, duty cycle, speed and control strategies on EMI level are considered.
The advantage of the recent countermeasures to mitigate EMI is that the improvement could be attained without adding any component or physical changes on the equipment hardware. On the other hand, it can be considered as cost-effective EMI mitigation technique. The common Pspice/Orcad 9.2 software is employed to simulate the effectiveness of some of the aforementioned countermeasures. Simulation results show the improvement in the performance of power electronics converters in EMC point of view.

2. Classifying Conducted EMI Mitigation Measures

In some of the EMI suppressing techniques such as filtering, snubbing, grounding and PCB modification, it is required to add some component or physical changes to the circuits. These kinds of measures are called hardware suppressing techniques. However, some countermeasures are based on switching characteristics of converters and it is not required to add any components to the circuit or any physical changes. Recent suppressing techniques are called software EMI mitigation measures. To be cost-effective is considerable advantages of software techniques.

3. Hardware Conducted EMI Mitigation Measures

A. Investigation of Filtering Effect on Conducted EMI

Filtering is the most effective and common measure to suppress conducted EMI [6]. In power electronic circuits, filters are placed both at the input and output of the converters. Isolation of the source from harmonic currents at the input and preventing voltage or current fluctuations at the output are performed by filters [7]. The same input and output filters could considerably improve the level of EMI in power electronic circuits. To have the best characteristics in relation to EMI, filters must be

designed based on special considerations and procedures, which is not the main object of this study.

In order to study the EMI, a simple and typical single-phase diode rectifier with no filtering circuit is chosen as depicted in Fig. 1. A Line Impedance Stabilization Network (LISN) is placed between the source and converter to provide the ability of conducted EMI measurement [4]. The parameters of different parts of the circuit are presented in appendix I.

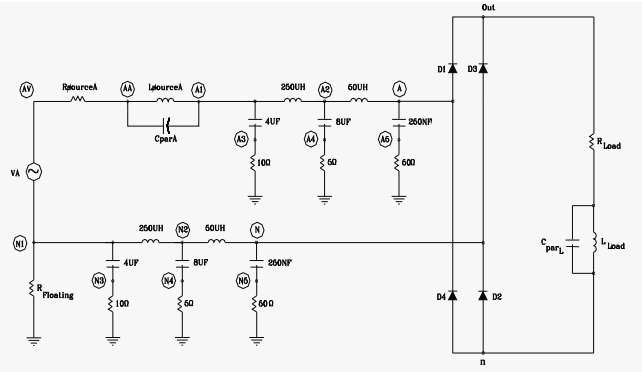

Fig. 1. Circuit diagram of a single diode rectifier with LISN

Simulation of the given circuit is performed using Pspice/Orcod 9.2 software. Spectrum of EMI at the output of LISN is the criterion of compliance with EMC regulation [4]. Comparing the LISN output simulation results of Fig. 2 with EMC regulations stated incompliancy.

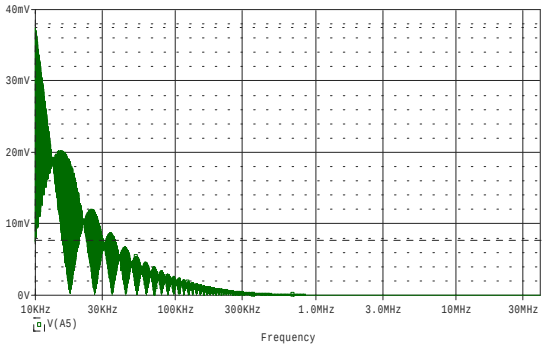

Fig. 2. EMI simulation results of single phase diode rectifier

Application of typical and common filters [7] at the input and output of the given circuit is studied.

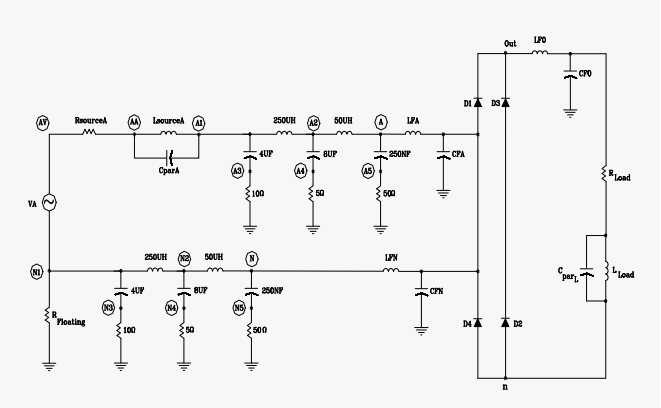

Fig. 3. Circuit diagram of single phase diode rectifier with input and output filters

Simulation repeated based on the new topology of the rectifier (as shown in Fig. 3) and filter parameters presented in appendix I. Fig. 4 shows the simulation results where considerable improvement in EMI level is observed.

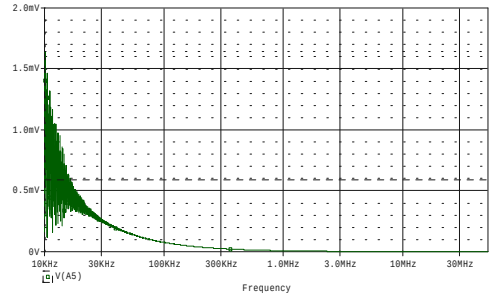

Fig. 4. EMI simulation results of single phase diode rectifier with input and output filters

B. Effects of Snubbers on Conducted EMI Level

High and rapid changes of voltage (*dv/dt*) and current (*di/dt*) in power electronic circuits imposes high tensions and stresses on semiconductor switches and in some cases corruption may occur [1]. Dissolving the matter by different topologies of snubber circuits is possible. Snubber circuits limit the rate of changes in voltages and currents on semiconductor switches [7]. Simulation of EMI due to the operation of a Buck type DC/DC converter is presented in [4]. The mentioned simulation is repeated for the same converter by applying a RC snubber circuit (with parameters given in App I) to protect the semiconductor switches. New topology of the converter is depicted in Fig. 5 and simulation results are shown in Fig. 6.

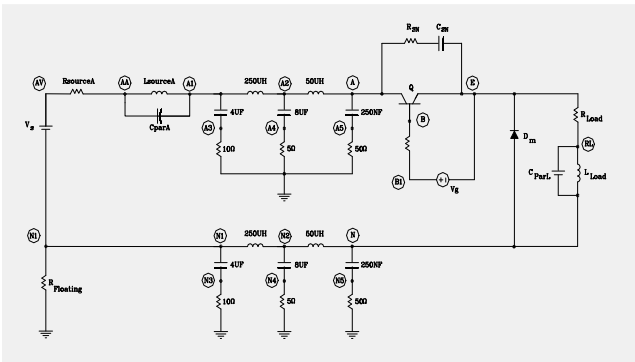

Fig. 5. Circuit diagram of a Buck DC/DC converter with RC snubber

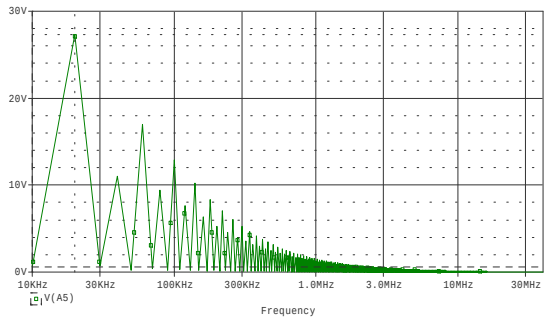

Fig. 6. Simulation results of Buck DC/DC converter with sunbber circuit

The improvement effect of the snubber circuit on the conducted EMI level is observed at odd harmonics of switching frequency and more improvement is attained at higher frequencies. It can be interpreted that the energy of interference signal is distributed over more extended frequency range [8] providing an effective reduction in EMI level. It is therefore concluded that controlling and limiting high variations of voltage and currents leads to lower EMI level.

C. Effects of Grounding on EMI Level

If different loads supplied by a common source, variation of each load imposes a disturbance to the other loads. Fig. 7 demonstrates two loads (Z_{L1} and Z_{L2}) supplying by one source (E). Z_s, Z_b, Z_g are source, bus and ground impedances of the system respectively.

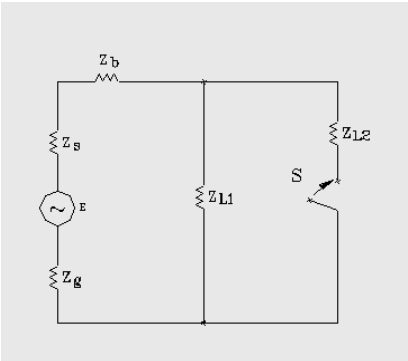

Fig. 7. Supplying two loads with a common source

Variation of Z_{L2} is modeled by operation of switch S. With the assumption $Z_{L1} >> Z_{L2}$ when the switch S is open the voltage variation on the Z_{L1} (ΔV) can be simply calculated as:

$$\Delta V = \frac{E(Z_g + Z_s + Z_b)}{Z_g + Z_s + Z_b + Z_{L1}} \qquad (1)$$

When the switch S is closed ΔV is calculated as:

$$\Delta V = \frac{E(Z_g + Z_s + Z_b)}{Z_g + Z_s + Z_b + Z_{L2}} \qquad (2)$$

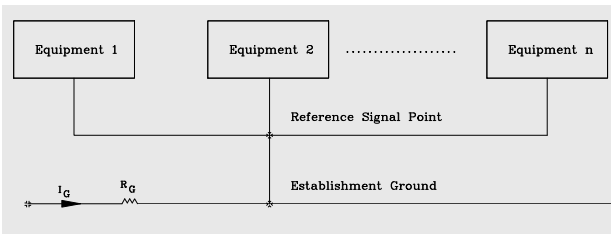

Fig. 8. Suggested grounding configuration

Therefore, ΔV on Z_{L1} fluctuates due to variation of Z_{L2}, which is not desired in most practical applications. In ideal conditions where Z_g, Z_s and Z_b are zero, $\Delta V=0$. In practical situations voltage disturbances (ΔV) can be minimized by minimizing Z_g. In other words, ΔV can be reduced by a better grounding in the system.

There are different grounding configurations [9-10], a common case is shown in Fig. 8. In this grounding technique, the ground of each equipment is connected to only a single point. This node is called reference signal point and connected to the earth. In this way the effect of establishment current on reference points is reduced [9].

D. Effects of PCB or Layout on EMI Level

PCB is the hidden aspect of electronic circuits design. It has considerable effects on performance of electronics circuits in EMC point of view. In PCB designing, it is necessary to pay attention to the following issues to retain EMC requirements [10-11]:

1) Analog and digital parts of the circuit in layout must be taken apart and have separated own grounds connected in a single point as the signal reference.

2) High frequency and low frequency sections of the circuit must be separated in order to decrease coupling effects.

3) High power and low power sections of the circuit and high and low current paths must be kept as far as possible to reduce coupling effects.

4) Traces especially sensitive ones must be short, thick and wide to have minimum resistive impedances.

5) Traces for sensitive signal and return paths must be kept as close as possible to reduce mutual inductance and inductive impedances.

6) Conducting loops must be avoided because current carrying loops perform as an antenna, which are the sources of EMI.

7) If cost is not a limitation, it is better to use PCBs with at least four layers in which two layers are assigned to power supply and grounding system. In this case, source and ground impedances are reduced considerably. Power supply and ground layers in a four-layer PCB act as shielding plates and prevent incoming and outgoing EMI. In two-layer PCB applications, the unused parts of the layers must be left full of copper and connected to the ground.

8) Traces of sensitive signals could be placed between two stable tracks so that they act as shield for them.

9) Considering some capacitors in PCBs to reduce the area of current carrying loops and disturbances in different parts of the layout is recommended.

10) Placement of bulk capacitors on supply traces is also advised to reject conducted common mode [4].

Fig. 9 shows a two-layer PCB of a Boost type DC/DC converter [12]. In this figure solder layer (top) and component layer (bottom) are separated. Almost all of the aforementioned considerations are considered where

favorite performances are obtained as compared to the other PCB designs [12].

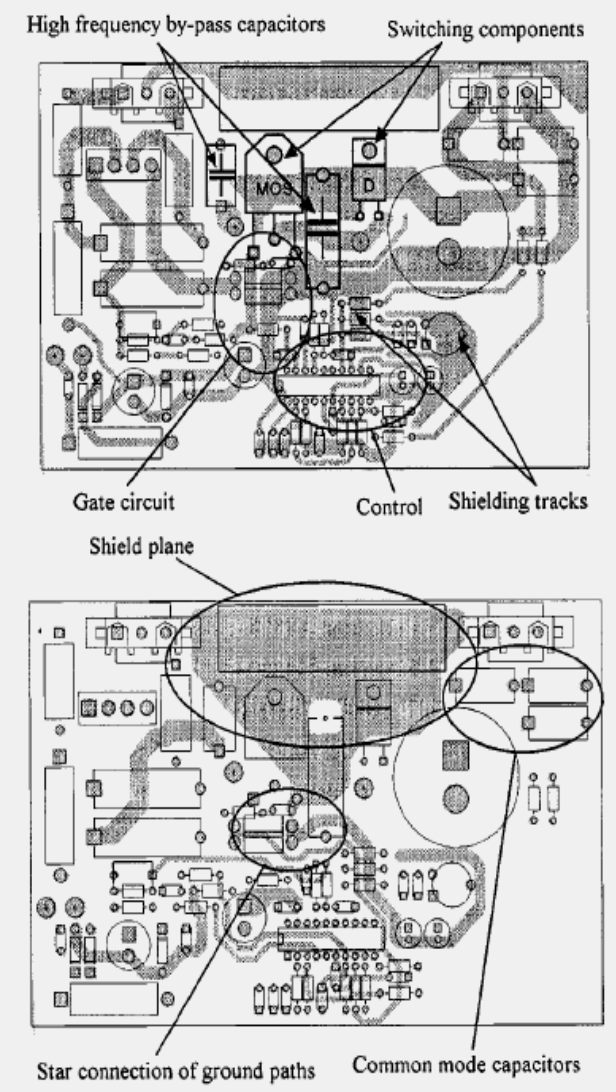

Fig. 9. PCB layout of a Boost Converter: solder layer (top) and component layer (bottom) [12]

4. Software Improvement of Conducted EMI

For software category of EMI mitigation techniques, no physical changes or adding components are required for the power electronic circuit. Frequency, speed, duty cycle and pattern of semiconductor switching equipment are the most effective parameters to reduce EMI.

A. Effects of Switching Frequency

Simulation results of conducted EMI for a Buck type DC/DC converter are presented in [4] where a fixed switching frequency of 20kHz and a duty cycle (D) of 0.5 was chosen. The simulation is repeated for the same circuit with switching frequency of 10kHz and 40kHz with the same duty cycle (ie D=0.5). Simulation results which are shown in Fig. 10 and Fig. 11 demonstrated a better EMI level when lower switching frequencies are used. However, it is against the advantages of using high switching frequencies in power electronic converters. Higher efficiency, lower size and weight of the system are among of these advantages [1]. This clarifies the importance and critical role of electronic designers to compromise and make appropriate decision.

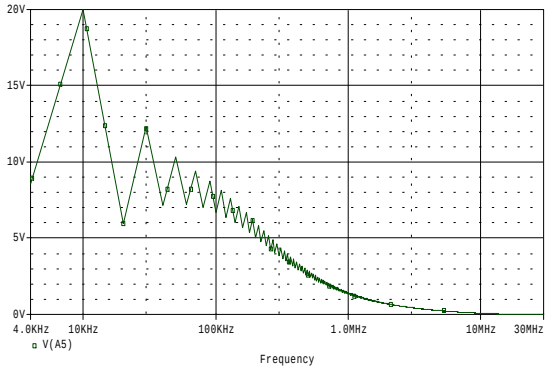

Fig.10. Simulation results of Buck DC/DC converter with 10 kHz switching frequency

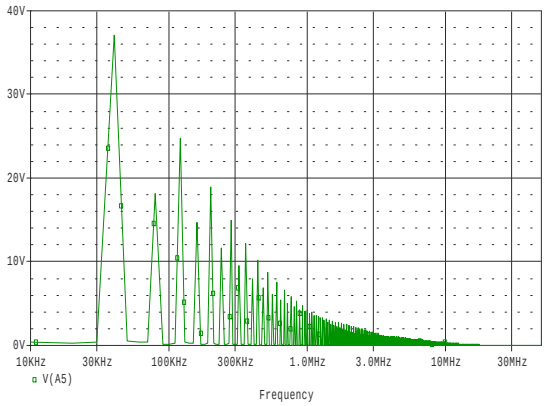

Fig.11. Simulation results of Buck DC/DC converter with 40 kHz switching frequency

B. Effects of Switching Speed

Rise time (t_r) in switching waveforms determines bandwidth (BW) of the system [13] as:

$$\mathrm{BW} = \frac{2.2}{t_r} \qquad (3)$$

The less rise time results in more bandwidth and possibility of higher frequency stimulation increased [13]. On the other hand, high rise time results in less stimulated frequencies and better EMI Level. Simulation is conducted for the same Buck type DC/DC converter of reference [4] for $5\,ms$ rise time. Simulation results are shown in Fig. 12 where less conducted EMI level is obtained for slower switching.

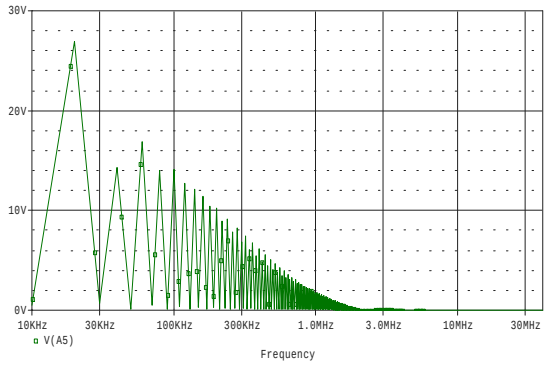

Fig.12. Simulation results of Buck DC/DC converter with $t_r = 5\,ms$

C. Effects of Duty Cycle

Comprehensive and analytical investigations about the effect of duty cycle on conducted EMI are studied in [14]. Fig. 13 and Fig. 14 show the simulation results for the Buck type DC/DC converter of reference [4] with D=0.25 and D=0.75 respectively.

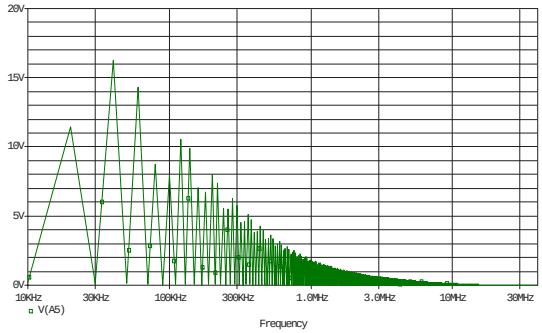

Fig.13. Simulation results of Buck type DC/DC converter with D=0.25

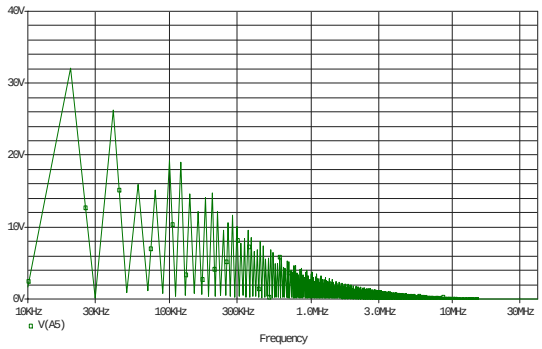

Fig.14. Simulation results of Buck type DC/DC converter with D = 0.75

The simulation results are compared with the results of the reference case with D=0.5 in point of view of EMC. For D=0.25 the even harmonies of switching frequency are increased and for D=0.75 the odd harmonics of the switching frequency are increased. However, in both cases other harmonics contents are decreased as compared with the reference case. In this case energy of EMI is distributed over more extended region in frequency domain [14]. It is clear to have lesser EMI energy in the range of frequency determined by the EMC regulations. In terms of EMC, the worst value for duty cycle of semiconductor switching is D=0.5. Decrement or increment of D provides better EMC levels.

D. Effects of Switching Strategy

Several switching control strategies are presented by professionals where the most common one is known as Pulse Width Modulation (PWM) [1, 7]. Simulation of three-phase full controlled rectifier is conducted and the results are presented in reference [4]. Implementation of PWM on this converter with 24 pulses per cycles and modulation index M=0.6 as the switching control strategy is considered [7]. Fig.15 and Fig.16 show the circuit diagram of the simulated converter and EMI simulation results respectively.

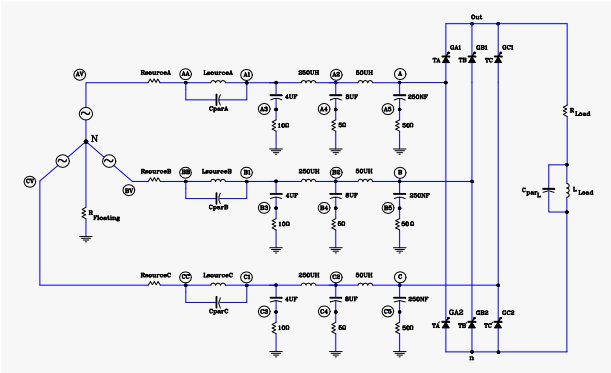

Fig. 15. Circuit diagram of 3-phase PWM controlled rectifier

It is concluded that, in spite of its advantages, EMI level becomes worse by applying PWM control strategy. Again the role of designers in compromising between different options and making the best decision is clear from the given results.

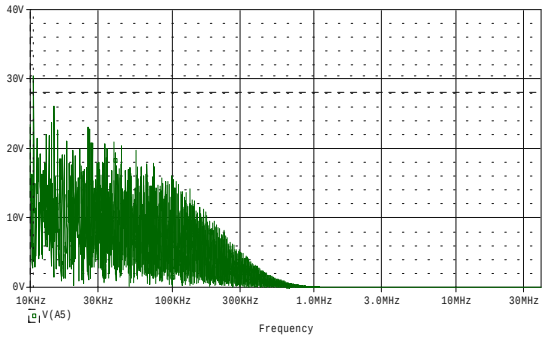

Fig. 16. Simulation results of PWM controlled AC/DC rectifier

5. Conclusion

Application of high frequency and high-speed semiconductor switches in power electronic circuit is increasing more and more. Power electronic circuits are the sources of Electromagnetic Interference (EMI) and they are mostly not in compliance with Electromagnetic Compatibility (EMC) regulations. Thus, it is required to reduce and limit of EMI level. The mitigation methods are classified in two hardware and software categories. Performance of these two categories of EMI reduction has been investigated in this paper by means of simulation.

The first method of EMI reduction is performed by some physical changes or adding components to the power electronic circuits. Filtering, snubbing, grounding and Printed Circuit Board or layout design are analyzed as the samples of measures in this category. In the second category no physical changes or adding components are required. Frequency, speed, duty cycle and control strategies of semiconductor switching devices have been investigated in this paper as the samples of software EMI suppressing techniques. Effects of these issues on EMI level due to the operation of several PE converters such as diode rectifier, dc/dc and ac/dc converters have been studied in this paper. Pspice/Orcad 9.2 software has been employed for the simulation of the given circuits. For each circuit, the compliance with EMC regulations has also been studied with and without applying mitigation techniques. It is concluded that soft switching is preferred to hard switching for better EMC.

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Appendix I

1) Simulated diode rectifier parameters:

RMS input Voltage	220V
Frequency	50Hz
Load impedance	3.18Ω
Load angle	$\cong 80^{\circ}$
$R_{\mathbf{sourceA}}$	0.1mΩ
$L_{source\ A}$	100nH
C_{parA}	2pF
C_{parL}	2pF
$R_{floating}$	1E12Ω
L_{FA}	1mH
C_{FA}	$10mF$
L_{FO}	10mH
C_{FO}	$30mF$

2) Simulated DC/DC Converter parameters:

V_s	110V
R_{source}	0.1Ω
L_{source}	10nH
C_{pars}	2pF
R_{load}	6Ω
L_{load}	$50mH$
C_{parL}	2pF
$R_{floating}$	$1E12\Omega$
R_{SN}	100Ω
C_{SN}	$10mF$

3) Simulated AC/DC Converter parameters:

RMS input Voltage	220V
Frequency	50Hz
Load impedance	1.5Ω
Load angle	30°
$R_{sorce\ A,B,C}$	$0.1m\Omega$
$L_{source\ A,B,C}$	100nH
$C_{par\ A,B,C}$	2pF
C_{parL}	2pF
$R_{floating}$	$1E12\Omega$