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Design of a control strategy for a three-phase DC/AC electronic converter to supply virtual inertia from a renewable energy source connected to the unbalanced electrical grid.

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Abstract. Power electronic converters play a critical role in the integration of renewable energy sources, especially in distributed generation systems and microgrids. They must operate safely and efficiently under all operating conditions, particularly in unbalanced grids. The provision of virtual inertia using simple and efficient control algorithms represents a good alternative to improve the stability of distributed generation systems. This article proposes the design of a control strategy to provide virtual inertia from renewable energy sources connected to unbalanced power grids using the PLL (phase tracker system) as an element for estimating the phase and frequency of the voltage wave and applying appropriate tuning of the controllers to take advantage of the system dynamics.

Key words. Electronic converter, phase-locked loop (PLL), renewable energy, second harmonic filter, unbalance grid, virtual inertia.

1. Introduction

The electrical system is by nature unbalanced, especially in distributed networks consisting of three-phase supply and single-phase loads.
Today is popular the use of PLL in Grid Following strategy to control the power coming from the renewable source. The typical scheme contemplates the use of the PLL for the estimation of the network phase and frequency, using a cascade control system with current and voltage loops associated with a control for the supply of virtual inertia.

The controller is implemented in the dq0 coordinate environment, by means of Clarke and Park transforms, which allow the three-phase system of time-varying currents, voltages and powers to be decoupled to a time-invariant system with continuous values (such as a dc system).

However, in unbalanced systems the dq0 transform presents oscillations that affect the control system requiring the application of advanced and complex structures for grid synchronization in distributed generation controls such as decoupling network "DDSEF-PLL" [12], as well as the comparison with frequency tracking systems "FLL" [7], which represent an increase in the computation time and cost of the electronic components.

This article explores the use of the PLL as a synchronization element with the electrical network, applying a control strategy that optimizes its use under voltage imbalance conditions, allowing virtual inertia to be supplied efficiently, with significant savings in computing time and cost for its implementation.

The second section presents the criteria for the evaluation of unbalanced systems, the dynamics of the system against different levels of unbalance voltage and defining operating ranges applicable to the use of the PLL.

The third section presents the control strategy, which is based on previous works [1, 2], evaluating its performance and proposing a control system applicable to unbalanced systems.

The fourth section describes the design of the band-stop filter used to optimize the operation of PLL and evaluates its performance under unbalanced conditions.

2. Amplitude and Phase-voltage unbalance in three-phase systems

The NTCSE [4] specifies that "The phases of all three-phase systems must be balanced and equalized at all times."

Phase-voltage unbalance affects the operation of machines such as electric motors and generators, which is why current regulations establish the thresholds or limits of voltage imbalance to be taken into consideration. Table 1.

STANDARD	VOLTAGE UNBALANCE FACTOR (VUF)
IEC 60034-1	1%
IEEE 1159	2%

Table 1. Voltage unbalance limits.

For the analysis, an unbalanced three-phase network was modeled with deviations in amplitude and phase as shown in Table 2 and Figure 1.

Phase	Balanced Peak Voltage (V)	Unbalanced Peak Voltage (%)	Unbalanced Peak Voltage (V)	Unbalanced phase angle deviation (deg)
Va	179.6	5	188.6	0
Vb	179.6	-5	170.6	-10
Vc	179.6	0	179.6	-5

Table 2. Unbalanced voltage supply network in both amplitude and phase.

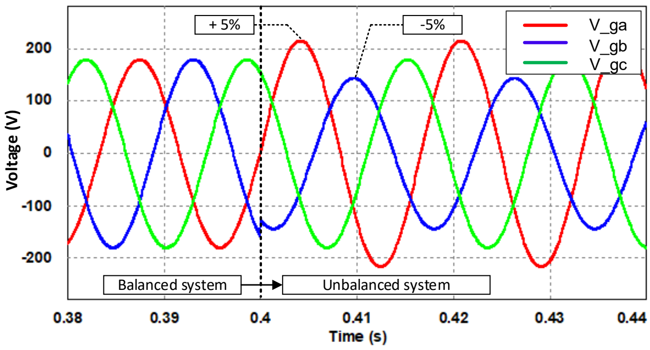

Figure 1. Unbalanced voltage waveform.

In (1) the "Voltage unbalance factor VUF" was determined as a proportion of the negative and positive sequence components of the system [6]

$$\text{VUF} = \frac{\text{negative−secuence voltage}}{\text{positive−secuence voltage}} \tag{1}$$

$$\text{VUF} = 2.89\ \%$$

By applying the dq0 transformation to the unbalanced voltage system, the presence of oscillations with an angular frequency of 2ω rad/s is observed. The negative sequence component appears in the positive sequence as a second harmonic at 120 Hz and the positive sequence component appears in the negative sequence at the same frequency. Figure 2.

It is evident that the control system proposed in this research operates adequately with a voltage imbalance of 5% and even with 10%, after which it goes out of control (20% unbalanced).

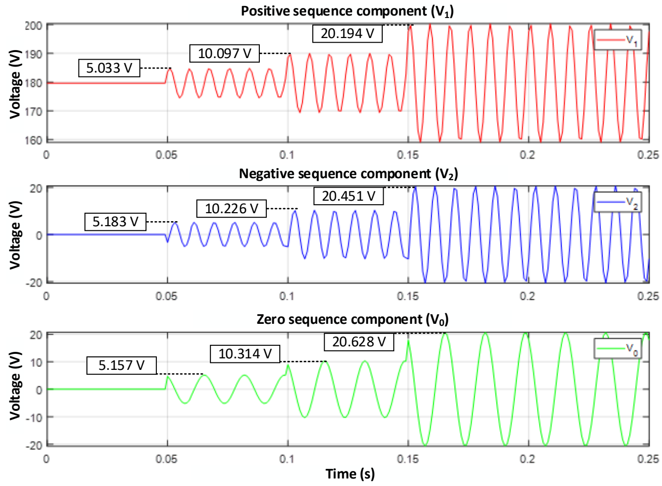

Fig. 2. Sequence components (dq0)

Performing the Fourier analysis shows the distortion of the voltage wave which contains a high second harmonic content. Figure 3.

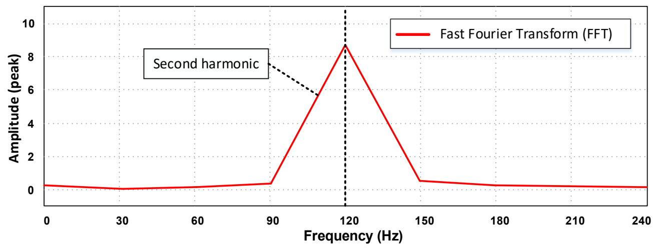

Figure 3. Identification of the second harmonic in the dq0 voltage components

3. Control strategy

The DC/AC converter control aims to regulate the DC bus voltage, maintaining the balance between the power supplied by the renewable energy source and the electrical grid.

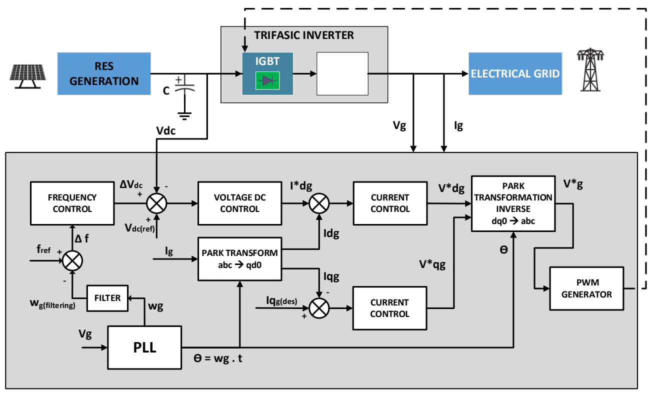

Fig. 4. Block diagram of the Grid-following inverter.

The proposed control strategy is based on the tuning of four controllers. The first controller corresponds to the PLL, whose design allows estimating the phase and frequency of the voltage wave in the supply network and at the same time limits its speed so that it can be followed by the voltage controller.

The second and third comprise cascade control with two independent control loops. A first Vdc voltage control loop that regulates the injection of active power by the renewable energy source and a current loop that stabilizes it, allowing the switching signals of the rectifier bridge in the inverter to be generated.

Finally, the fourth controller corresponds to the inertia loop, which regulates the discharge of static energy stored in the DC bus capacitor. Figure 4.

PLL control loop

For the present investigation, a PLL based on the phase-locked loop topology in a synchronous reference system (SRF-PLL), studied in [1]-[2], was modeled, whose block diagram is presented in Figure 5.

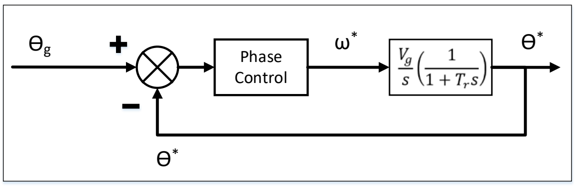

Figure 5. Block diagram of SRF-PLL [1].

The PI controller design for the PLL was developed using the symmetric optimum method with different cut-off frequencies. At t = 0.4 s, when the voltage unbalance is generated, oscillations with a frequency of 120 Hz are observed.

As the cut-off frequency is varied, the controller acts as a filter that limits the distortion generated by the unbalance. Obtaining the best result at w_c = 10 Hz, reducing ripple from 3% to 0.45%. Figure 6.

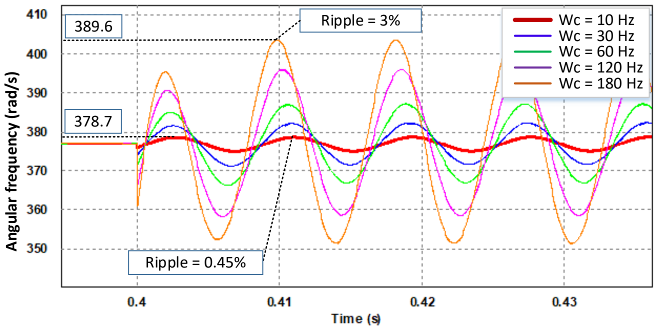

Fig. 6. Controller action on the distortion generated by voltage unbalance

The phase estimation controller is intentionally slow so that it can adjust to the speed of the voltage loop, which by nature has reduced bandwidth. The controller takes about 3 cycles to reach the true phase value (90 degrees of phase shift). Figure 7.

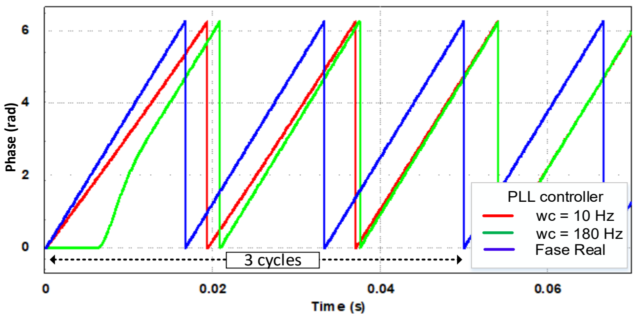

Figure 7. PLL behavior in phase tracking.

Current control loop

The simplified transfer function for the implementation of the current control loop is defined in [1]. Fig. 8.

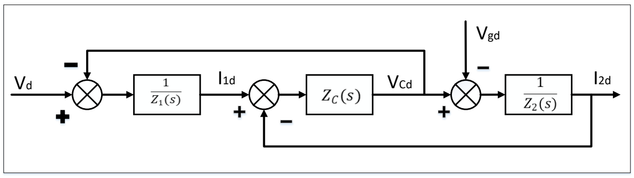

Fig. 8. Simplified block diagram of the LCL filter (plant) in the current control loop [1].

For the design of the current controller, the frequency method was used, evaluating the system response to different cutting frequencies. Fig. 9.

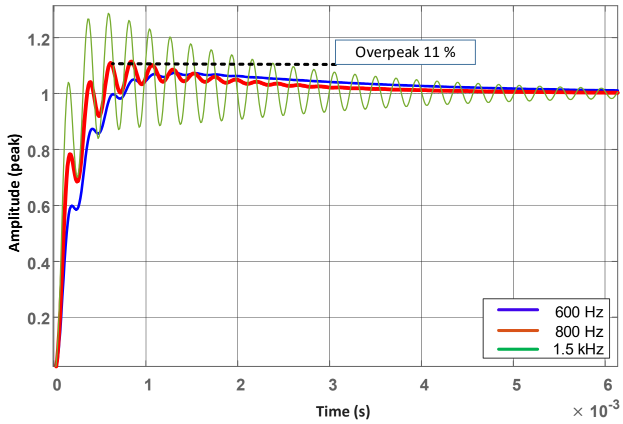

Figure 9. Current controller response with different cut-off frequencies.

The current controller design was carried out by evaluating the response to a unit step, selecting a cut-off frequency wc = 800 Hz.

Voltage control loop

From what is presented in [1] the transfer function of the plant is determined for voltage control on the DC bus. Fig. 10.

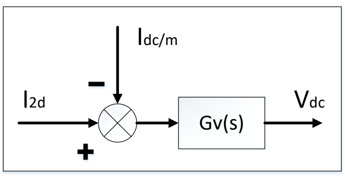

Figure 10. Block diagram of the voltage loop transfer function.

The transfer function $G_v(s)$ is defined by (2), where "m" is the modulation index and "C_{dc}" is the DC bus capacitance (2).

$$G_v(s) = -\frac{m}{sC_{dc}} \qquad (2)$$

The voltage loop on the DC bus has a reduced bandwidth and since it takes the voltage on the DC bus as an input signal, and considering that the voltage variations on the DC bus are proportional to the frequency variations, the voltage controller has to be synchronized so that its dynamics allow it to follow the frequency variations coming from the PLL, which is configured with a cut-off frequency of 10 Hz.

Since the inner loop is designed with wc = 800 Hz, the outer loop is designed at a speed less than one tenth of this, determining wc = 60 Hz.

The response of the voltage controller to a current step is presented in Figure 11.

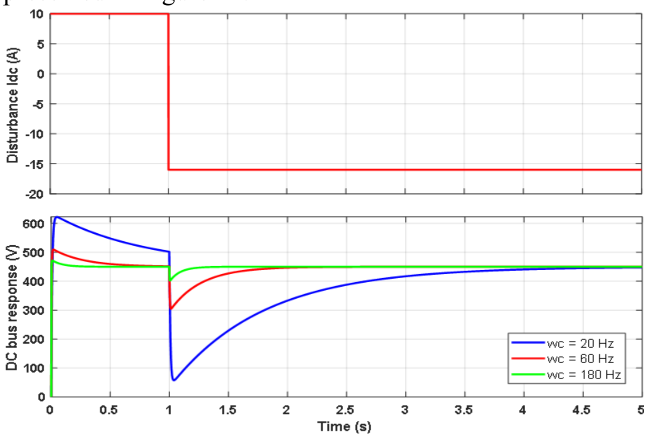

Figure 11. Time response with step from 10 to 16 A

Frequency control loop

The injection of virtual inertia into the system is carried out by controlling the discharge of static energy stored in the DC bus capacitor.

The frequency control loop consists of a proportional "P" controller used to scale the frequency and voltage signals, allowing the injection of virtual inertia to be controlled within the operating limits established for safe operation.

The DC bus is regulated at Vdcdes = 450 V, establishing the maximum voltage and frequency variation at $\Delta V = 25$ V and $\Delta f = 0.2$ Hz respectively. With these parameters, the proportional gain Kp = 125 is determined.

Table 3 presents the parameters that define the implemented control system.

Loop Control	Gain crossover frequency (Hz)	PI Parameters	
		Kp	Ti
PLL controller	10	0.3498	0.6333
Loop curren controller	800	5.3088	0.002
Loop voltage controller	60	-0.17	0.2653
Loop inertia controller	-	125	-

Table 3. Control system parameters.

4. Design filter stopping band

The use of the PLL as a synchronization element with the grid presents limitations regarding the tracking of the grid frequency, due to the presence of the second harmonic generated by the voltage unbalance.

Based on this, the use of a filter for the attenuation of the second harmonic present in the measurement of the grid frequency is proposed.

The implemented filter consists of three stages:

Filter	Cut-off frequency (Hz)	Center frequency (Hz)	Stopping Band (Hz)
1st-order low-pass filter	10	-	-
2nd-order Band-stop Filter	-	60	6
2nd-order Band-stop Filter	-	120	60

Table 4. Table 4. Band-stop filter design parameters.

The proposed control system uses the PLL as an element for frequency estimation, which is used as an input signal in the inertia controller. As observed in section 3, the designed controller acts as a filter, significantly reducing the influence of the second harmonic generated by voltage unbalance. Thus, in an unbalanced system, the implemented control presents a frequency tracking with a variation of $\Delta f = \pm 0.33$ Hz without the implementation of the filter, going to $\Delta f = 0.03$ Hz with the use of the band rejection filter. Figure 12.

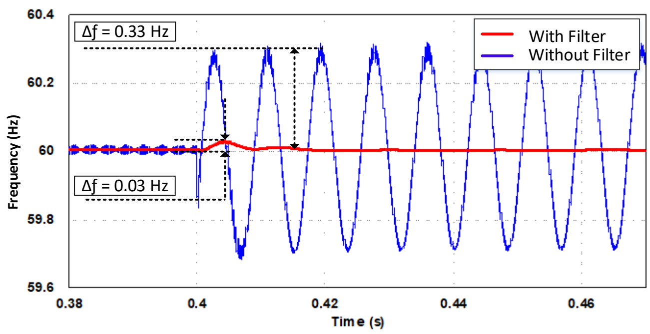

Figure 12. Improvement of the PLL in frequency tracking in unbalance conditions with and without filter.

Likewise, the implementation of the filter allows to improve the stabilization of the reference current Id2ref, reducing its ripple from 1 A to 0.095 A. Figure 13.

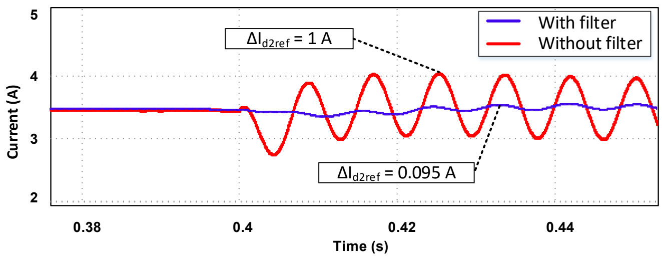

Figure 13. Effect of the rejection filter on the reference current.

5. Operation of the DC/AC converter under amplitude and phase unbalanced conditions.

This section analyzes the behavior of the control system for the injection of virtual inertia in the face of frequency variations under conditions of voltage imbalance in the supply network.

4.1. Operation of the DC/AC converter under amplitude unbalanced conditions

In this section the results are analyzed under conditions of magnitude unbalance.

The analysis was performed considering a frequency drop $\Delta f = 0.3$ Hz, with a rate of change of frequency (RoCoF) of -3 Hz/s, at time T = 0.8 s. Figure 14.

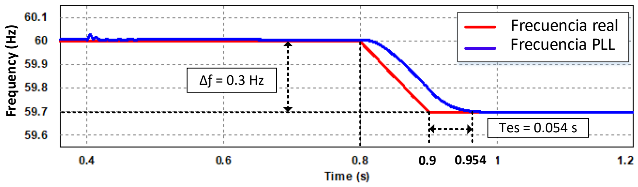

Figure 14. Frequency drop in the supply network.

DC bus voltage

By graphing the DC bus voltage, the system response to the frequency variation $\Delta f = 0.3$ Hz can be observed, observing the energy discharge carried out, which represents the virtual inertia supply in accordance with the graph of the effective active power presented in Figure 15.

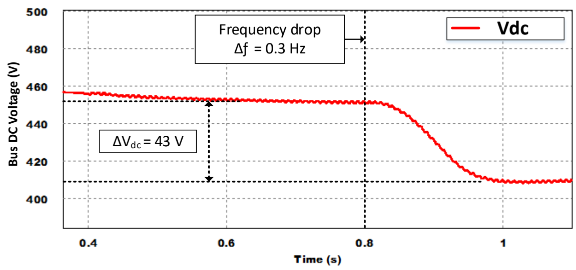

Figure 15. Bus dc voltage.

Active power

For the evaluation of results, the total active power of the system expressed in effective value is considered, which is composed of a first term that corresponds to the total active power of the system expressed in effective value and a second term that corresponds to the instantaneous active power due to the imbalance of the intensities [3].

The results obtained are shown in figure 16. Also, the decomposition of effective active and unbalance power is shown.

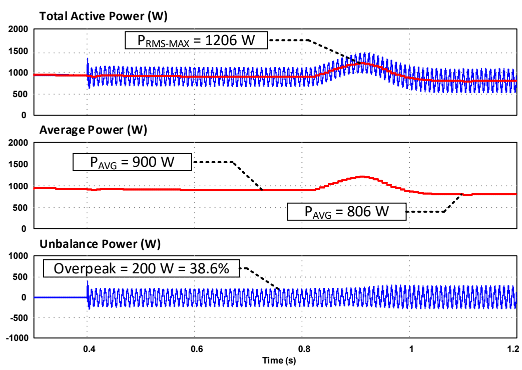

Figure 16. Total instantaneous power of the three-phase system

Current and voltage

In the case of the control system without the band-rejection filter designed in Section 4, a significant unbalance is observed in the three-phase current injected into the grid, accompanied by severe distortion in the phase "Ia" current waveform. Figure 17.

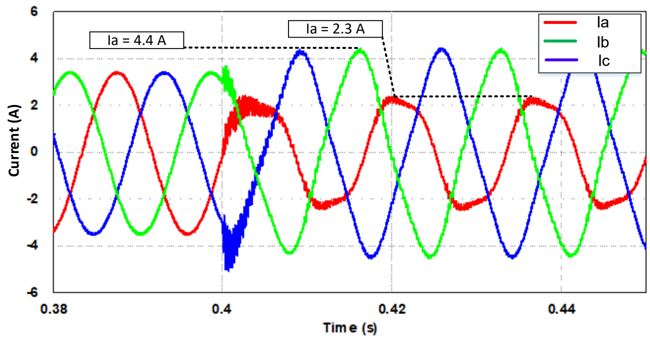

Figure 17. Three-phase current injected into the grid (without Filter stopping band)

With the implementation of the filter, the balance of the three-phase current injected into the network is partially improved, especially in phase “a” which was totally distorted as shown in Figure 18.

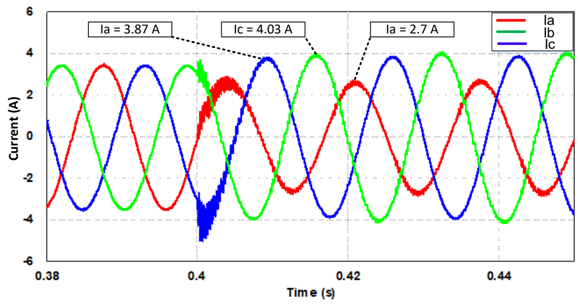

Figure 18. Three-phase current injected to the grid (with Filter stopping band)

4.2. Phase Unbalanced Conditions

For phase imbalance, deviations in phases "b" and "c" were considered, assuming $\Delta\theta_b = -10°$ y $\Delta\theta_c = -5°$ at time t = 0.4 s. The results are shown in Figure 19.
The PLL response to phase imbalance is observed as a transient that records a drop in the frequency recorded by the PLL.

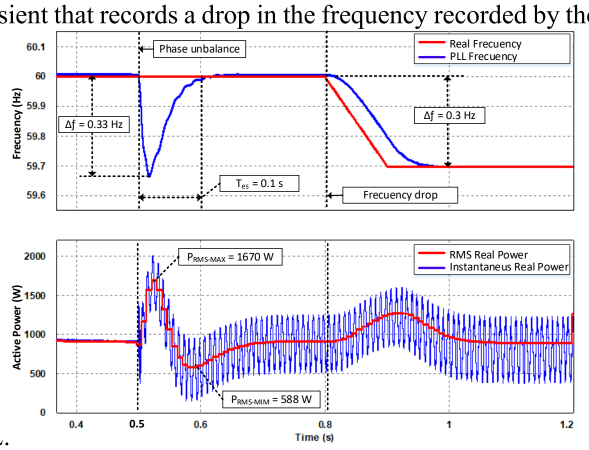

Figure 19. Virtual inertia control system responds under phase unbalanced conditions.

The introduction of phase imbalance generates a transient with a deviation in the phase angle estimate of ΔΘ = 5°. The virtual inertia control system responds to the generated transient by dispatching power from the DC bus, observing that the system provides support in the event of this contingency. This demonstrates that the system is robust to phase imbalance, including the transient portion.

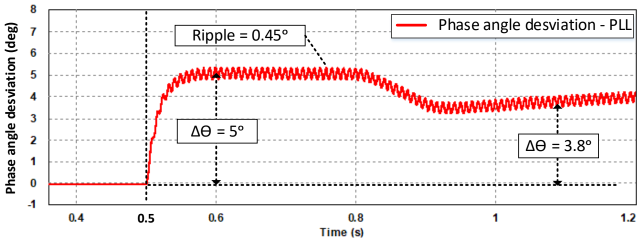

Figure 19. Virtual inertia control system responds under phase unbalanced conditions.

The phase tracking performed by the PLL is affected by the phase imbalance in the supply network. This behavior is considered normal, since the phase imbalance generates a delta of theta in the PLL control loop.

For future research, it is proposed to further study the behavior of the currents generated by the proposed phase imbalance.

6. Conclusion

This paper presents the design of a control strategy for a three-phase DC/AC electronic converter based on the use of the PLL as a phase and frequency tracking element, applied to unbalanced electrical systems in order to provide virtual inertia. The main contribution is the design of a low complexity control system, based on the tuning of the PLL, current, voltage and virtual inertia controllers to optimize its operation in unbalanced networks. The controller designed for the PLL acts as a second harmonic filter, facilitating the tracking of the frequency signal and allowing the operation of the control system under voltage unbalance conditions. Furthermore, the proposed second harmonic filter improves the stabilization of the reference current in the current loop, allowing to partially improve the waveform and balance of the current supplied to the grid.

Acknowledgement

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