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A Comparative Study of Non-Isolated Voltage Balancers Applied to Bipolar DC Microgrids

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Abstract. The imminent expansion of distributed generation by small-scale units associated with renewable sources - such as wind and photovoltaic – combined with the increasing penetration of electric vehicles, highlights the strategic importance of DC microgrids. These systems conventionally adopt two main configurations: unipolar or bipolar. Specifically, in bipolar DC microgrids, converters with multiple voltage levels or voltage balancer converters can be employed. These converters are designed to mitigate the effects between the network terminals, particularly under load imbalance conditions. Hence, this work aims to contribute to a comparative analysis of the main non-isolated voltage balancer topologies, highlighting key aspects such as efficiency, costs, voltage regulation, and current oscillations.

Key words. Bipolar DC microgrid, Non-isolated converters, Voltage balancer.

1. Introduction

Nowadays, most commercial and residential loads use a rectifier as the first energy conversion stage, converting the grid's AC voltage into a DC voltage [1], [2]. A DC microgrid can eliminate this stage, resulting in a more efficient system. Renewable energy sources (RES), such as photovoltaic (PV) and wind power, can be easily integrated into DC microgrids [3], [4], [5]. Moreover, the DC microgrid control is easier than that of AC grids, as it does not require managing parameters such as frequency and phase synchronization [3], [6]. DC microgrids can be divided into two types: unipolar and bipolar [7]. Unipolar microgrids can present one or more positive DC voltages. On the other hand, bipolar DC microgrids present positive and negative voltage levels, each one suited to specific applications. One of the most common configurations is ± 190 V, which is widely utilized in data center systems [3], [8].

Several topologies can be utilized to build a bipolar DC microgrid, highlighting the following structures [3], [9], [10], [11]: i) unidirectional DC-DC interface converter between a PV system and the microgrid, which is characterized as grid following and must harvest the maximum power in PV-array; ii) bidirectional DC-DC interface between battery energy storage system (BESS) and microgrid, responsible for controlling both charging and discharging processes of the BESS; iii) AC-DC unidirectional interface between the wind energy system and microgrid; iv) AC-DC bidirectional grid interface converter, which can utilize energy from the utility grid or inject active current into the grid when surplus power is available from local sources; v) unidirectional DC-DC converter, responsible for supplying loads that requires voltage level different from the main DC-link; vi) unidirectional DC-AC converter for supplying AC loads; vii) Voltage balancer, which equalizes the voltage between the positive and negative poles of the bipolar DC microgrid. This paper presents a comparative analysis of non-isolated voltage balancer topologies, which play a crucial role in the operation of bipolar DC microgrids. This study evaluates nine different topologies, highlighting some characteristics such as RMS current through the main components, power losses, and implementation costs for each topology.

2. Methodology

Voltage balancers deal with imbalances in a bipolar DC microgrid, using the maximum voltage in the DC link. Additionally, the electrical circuit must be able to avoid through-shoot problems, or strategies such as dead time can be employed. Topologies such as those presented in [12], [13], [14] mitigate through-shoot by employing electric components. The interleaved Buck-Boost in [12], the three-level converter in [9], [15], and the three-level Buck-Boost proposed in [14] employ four power switches and interleaved operating. Thus, each switch is turned on for a quarter of the switching period, reducing the conduction losses.

The analyzed topologies in this paper are organized in Fig. 1 while Table I presents the main obtained results, in which the topologies are classified as 1: Fig 1(a); topology 2: Fig. 1(b); topology; 3: Fig. 1(c); topology 4: Fig. 1(d); topology 5: Fig. 1(e); topology 6: Fig. 1(f); topology 7: Fig. 1(g); topology 8: Fig. 1(h); topology 9: Fig. 1(i)

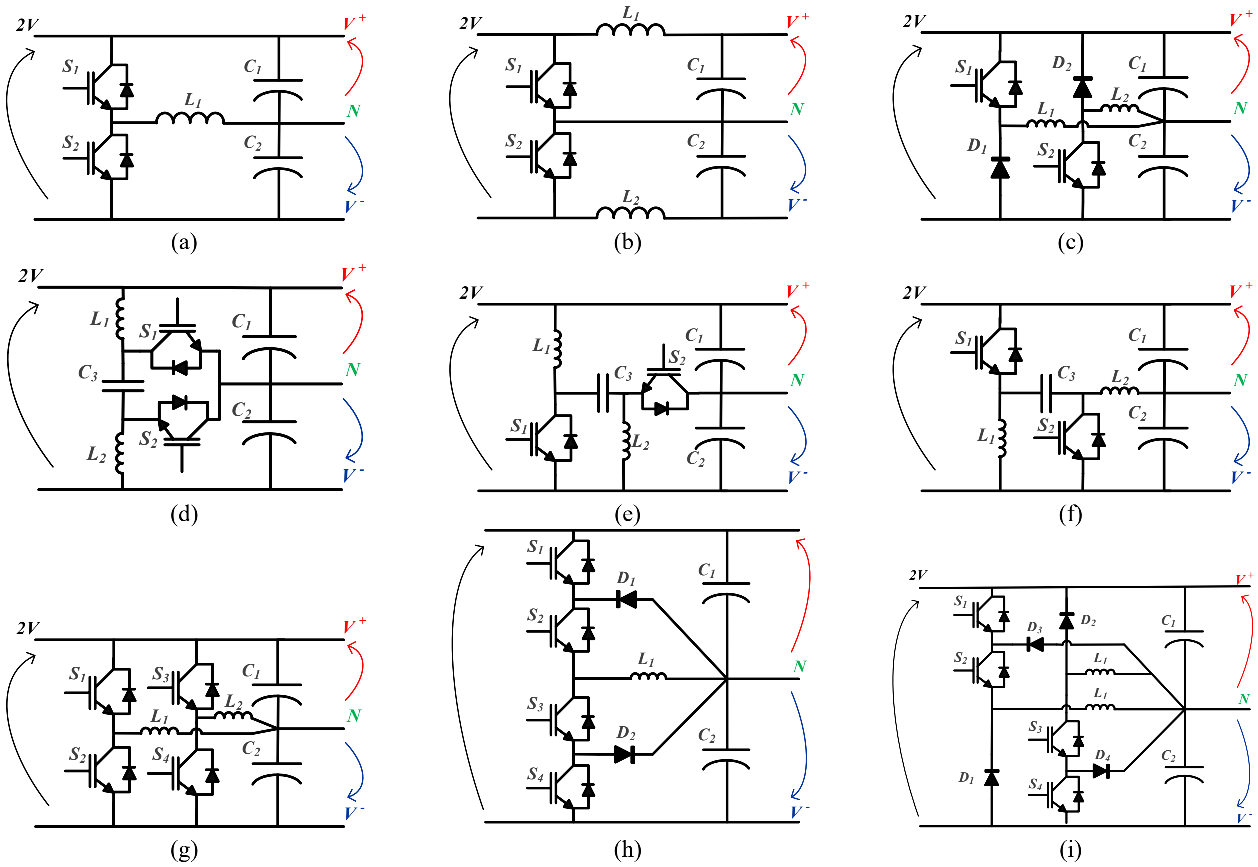

Fig. 1. Non-isolated voltage balancer topologies: (a) 1:Buck-Boost [16], [17]; (b) 2: Type 2 [18]; (c) 3: Dual-Buck Half-Bridge proposed in [13]; (d) 4: Ćuk [12]; (e) 5: Super-SEPIC [12];(f) 6: Super-Zeta [12]; (g) 7: Interleaved Buck-Boost [12]; (h) 8: Thee-level converter [9], [12], [15]; (i) 9: Three-level dual Buck-Boost proposed in [14].

This work employed a load imbalance of eight times to compare the topologies. Thus, the negative pole supplies a load of 226 W, using 160 Ω resistance, while the positive pole supplies a load of 1805 W, employing a 20 Ω resistance, totalizing a 2031 W system.
The passive components can be designed using the imbalance condition. Using topology 1, the average inductor current is calculated as the difference between the load currents by:

$$I_{L_1} = \frac{V_{C_1}}{R_1} - \frac{V_{C_2}}{R_2} = 8.3125\ A \qquad (1)$$

where R_1 represents the load in the positive pole, and R_2 represents the load connected to the negative pole.

In balanced configurations, the current through R1 is equivalent to the current through R2, causing, ideally, a null average current through the inductor. During the first operation stage, the voltage across the inductor is equivalent to Vin, i.e., 380 V. Considering a maximum ripple of 20%, a duty cycle of 0.5, and a switching frequency of 20 kHz, the inductance is calculated by:

$$L_1 = \frac{V_{in}D}{f_s \Delta I_{L_1} I_{L_1}} = 1\ mH \qquad (2)$$

Assuming the 1% voltage ripple in the poles of the microgrid and the equality between C1 and C2. The capacitance is obtained as follows:

$$C_1 = C_2 = \frac{V_{in}D}{8{f_s}^2 \Delta V_{C_1} I_{L_1} L_1} = 240\ \mu F \qquad (3)$$

Topologies 4, 5, and 6 employ a coupling capacitor, which can be calculated as:

$$C_3 = \frac{V_{in}}{f_s \Delta V_{C_3}(R_1 + R_3)} = 1.4\ \mu F \qquad (4)$$

A proportional-integral (PI) controller can control the voltage balancer topologies. However, the presented voltage balancers show some similarities, causing distinct PI-based control structures to be used. The topologies 1-6 employ two switches, which operate complementarily. Fig. 2(a) represents the control strategy for these topologies. Topology 7 utilizes an interleaved switching, where the pair S1 and S2 initially commute complementarily, and subsequently, the pair S3 and S4 commute complementarily, as shown in Fig. 2(b). Already, Fig. 2(c) represents the control strategy for the topologies 8 and 9, based on the three-level converter. In these topologies, the switches S1 and S3 are directly influenced by the control action, while the switches S2 and S4 depend on an additional delay.

The proportional and integral gains of the PI controllers are tunned based on the frequency response of the transfer function represented in (5). Choosing a crossover frequency at 12 Hz and a phase margin at 88º, the PI controllers' gains are obtained by Kp = 0.000103 and Ki = 0.1977. The obtained gains are employed in all topologies, independently of the control schematic utilized, as shown in Fig. 2. The adopted PI controller exhibits good steady-state performance across all topologies, guaranteeing the voltage balance. Additionally, the topologies use the same capacitance and inductance values, resulting in a similar frequency response.

$$G_{vd} = \frac{V_{in}}{2C_1L_1s^2 + L_1\left(\frac{1}{R_1}+\frac{1}{R_2}\right)s + 1} \quad (5)$$

3. Simulation Results

The voltage balancer topologies were analyzed and compared to each other by computational simulation using MatLab/Simulink® software. The entire simulation system was discretized, including the PI controllers.

For a better visualization, Table I organizes the results. All analyzed voltage balancer converters provide an elevated efficiency of over 97.7% despite the load imbalances. Topologies 4 and 5 are not symmetrical and use a duty cycle of around 0.3 in the switch S1. These topologies exhibit the highest voltage across the switches and the highest losses in these components. Topologies 8 and 9 show the lowest voltage level across switches. However, topology 7 presents the lowest switching losses. This topology employs an interleaved switching. The losses are obtained by simulation using the thermal model in the PSIM software, by utilizing the models for the IGBTs IRGP4650D and diodes 30ETH06 when necessary. Each inductor considers an internal resistance of 1 mΩ, which is associated with the conduction losses. The magnetic losses are disregarded.

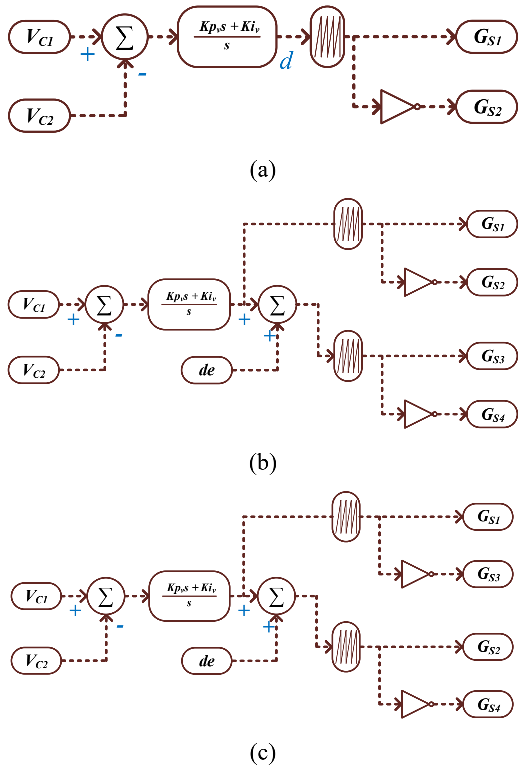

Fig. 2. PI-based control schematic: (a) Topologies 1-6; (b) Topology 7; (c) Topologies 8 and 9.

Table I. - The Main Results for Each Voltage Balancer

Top		V_{Smax} [V]	S_Loss [W]		V_{dmax} [V]	D_Loss [W]		I_{Lmed} [A]	I_{Lef} [A]	L_Loss [W]	T_Loss [W]	Effi [%]	Cost [pu]
1	S_1	380	5.39				L_1	8.31	8.42	0.85	21.47	98.95	1.00
	S_2	380	15.23										
2	S_1	380	5.7				L_1	9.50	9.60	1.11	22.50	98.90	1.31
	S_2	380	16.18				L_2	1.18	1.81	0.04			
3	S_1	380	8.16	D_1	380	1.23	L_1	2.32	2.69	0.09	36.23	98.25	1.45
	S_2	380	17.83	D_2	380	7.54	L_2	10.63	10.72	1.38			
4	S_1	380	15.4				L_1	4.13	4.42	0.23	21.06	98.97	1.43
	S_2	380	5.19				L_2	4.18	4.47	0.24			
5	S_1	570	29.23				L_1	4.11	4.52	0.25	36.96	98.21	1.43
	S_2	570	6.62				L_2	8.31	8.51	0.87			
6	S_1	570	29.45				L_1	4.01	11.24	1.52	41.84	97.98	1.43
	S_2	570	9.65				L_2	8.33	10.11	1.23			
7	S_1	380	2.16				L_1	4.16	4.38	0.23	27.88	98.65	1.74
	S_2	380	11.55										
	S_3	380	11.55				L_2	4.16	4.38	0.23			
	S_4	380	2.16										
8	S_1	190	5.14	D_1	190	0.48	L_1	8.75	8.86	0.94	36.32	98.24	1.57
	S_2	190	10.76										
	S_3	190	8.67	D_2	190	0.00							
	S_4	190	10.33										
9	S_1	190	5.48	D_1	380	0.64	L_1	10.92	11.00	1.45	45.81	97.79	2.03
	S_2	190	12.84	D_2	380	0.10							
	S_3	190	4.31	D_3	190	1.10	L_2	2.17	2.56	0.08			
	S_4	190	12.3	D_4	190	7.51							

Topologies 3 and 9 present the diodes' highest voltage and power losses. The voltage is around 280 V, whereas the losses are around 7.5. In the analyzed conditions, one of the diodes in topology 8 does not present power losses, as this component does not show current flow.
Topology 1 presents the lowest cost and is the simplest topology, employing few components, only two power switches, an inductor, and two capacitors, whereas topology 9 has the most elevated cost, as this topology is built by four power switches, four diodes, two inductors, and two capacitors.
Fig. 3 exhibits some simulation results. The PI controller was set to 12 kHz, resulting in a slow dynamic and requiring a relatively long simulation time for a fair comparison. Fig. 3(a) shows the positive and negative pole voltage for topology 3, where the PI controller employed can equalize the voltage levels. All topologies must achieve this behaviour. Fig. 3(b) compares currents through the inductors in topologies 1 and 2. Fig. 3(c) compares currents through topologies 5 and 7. Fig. 3(d) compares voltages and currents for power switches for three voltage balancer structures.

4. Conclusion

This paper presented an extensive comparative analysis of the most relevant non-isolated voltage balancer topologies, evaluating nine different structures that can be employed in bipolar DC microgrids to mitigate voltage imbalance issues. All topologies exhibited high efficiency under imbalanced load conditions. Notably, the Ćuk voltage balancer achieved the highest efficiency and provided equalized currents through the inductors. Additionally, this topology is not susceptible to shoot-through problems due to its structure. The Buck-Boost topology stands out for its simplicity, low implementation cost, and good overall efficiency.

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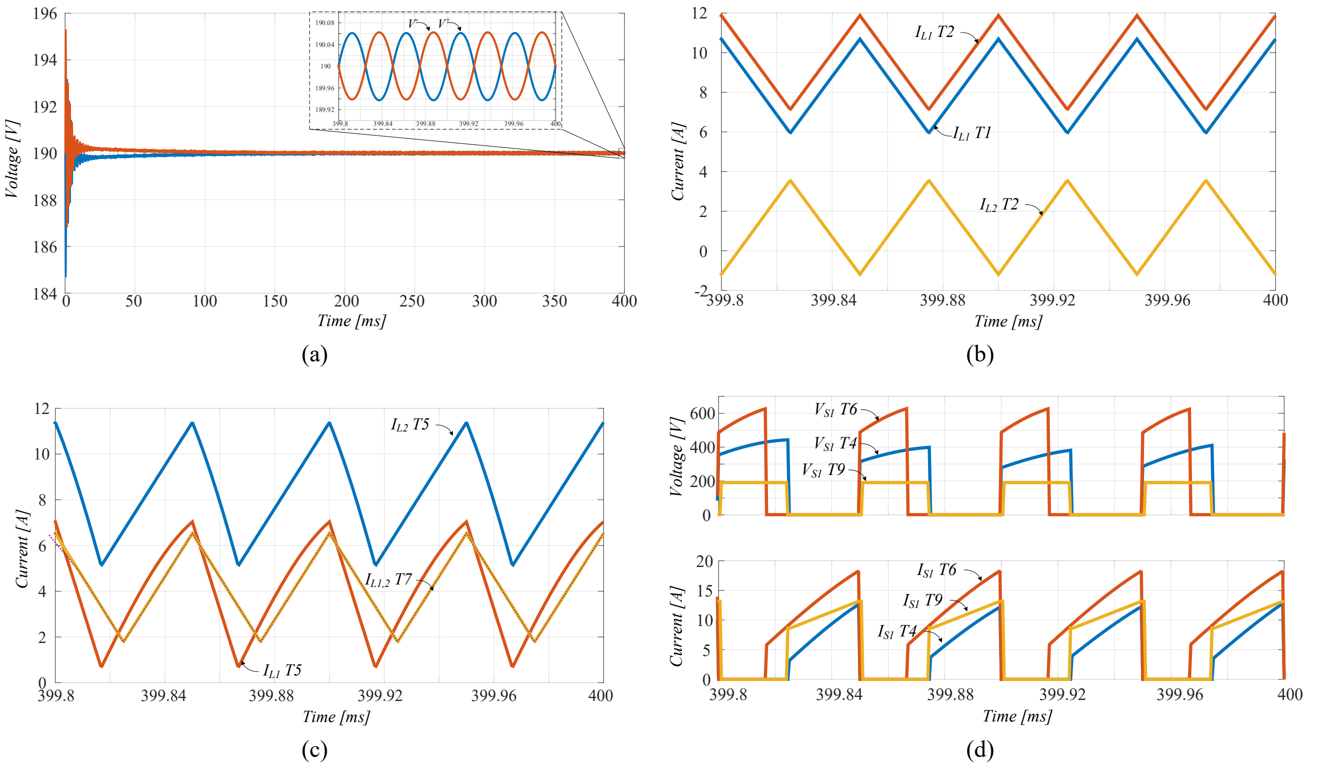

Fig. 3. Simulation results: (a) Positive and negative pole voltage for topology 3; (b) Currents through inductors in topologies 1 and 2; (c) Currents through inductors in topologies 5 and 7; (d) Voltage and current for power switches in topologies 4, 6, and 8.

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