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Detailed Simulation and Loss Estimation of Active-Clamped ZVS Current-Fed Full-Bridge Isolated DC/DC Converter

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Abstract. Estimating losses and efficiency of power electronic converters requires accurate simulation models of all components. Detailed computer simulation involves determining inductor currents and capacitor voltages using a solver for ordinary differential equations. However, solvers do not work well if the system is complicated and has very small time constants caused by snubber circuits. In current-fed topologies this is often the case, and certain snubber circuits may not be easily eliminated as the circuit does not work without them even if all other components are considered ideal. Detailed simulation of such systems is not straight forward. Better results could be obtained by using a minimalistic model which uses ideal components and only contains the most important elements of the power circuit. Waveforms generated from such a model can then be further post-processed to generate the waveforms of real components and to calculate losses. This paper presents such a solution for an active-clamped ZVS current-fed full-bridge isolated DC/DC converter topology.

Key words. Simulation, Loss Estimation, Current-Fed

1. Introduction

In the industry it is often required to perform analysis and identify possible points of improvement on older hardware designs using modern technologies. Even if a complete redesign of the hardware is not possible for economic reasons, major improvements in efficiency and reliability might be done with minor changes in hardware or control software. Detailed computer simulation can be used to estimate theoretical losses in various parts of the system. Comparison of simulation results of waveforms and calculated losses with measurements on actual hardware helps to identify additional problems and causes of losses in the circuit. These may be easily eliminated by a cheap fix in the design without significantly affecting the manufacturing process. In this paper, the lessons learned during such a process have been shown. Of significant importance are the simulation methodology used with a current-fed converter containing snubber circuits with short time constants.

A. Topology

The topology under discussion is the single phase Active-Clamped ZVS Current-Fed Full-Bridge Isolated DC/DC Converter, shown in Fig 1. This is an old topology and has already been published in the 1990s – early 2000s in [1] – [3]. The actual device which has been analysed via simulation is an AC/DC power supply for railway applications. It has been designed by PowerQuattro JSC in the 2000s [4]. A photo can be seen in Fig. 2. Input: 230V 50Hz single phase, output up to 375V 20A DC.

Fig.2. AC/DC power supply by PowerQuattro [4]

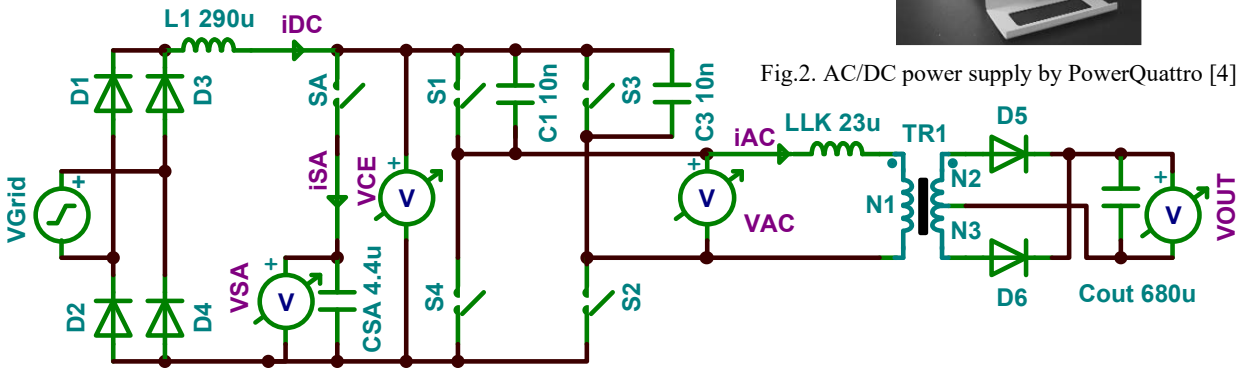

Fig. 1. Power circuit diagram of the simulated active-clamped ZVS current-fed full-bridge isolated DC/DC converter

Analysis [5]-[6] and small signal modelling [7] of the topology are already presented. A comparison with alternative topologies can be found in [8]. Further control advances using MOSFET based bidirectional switches for SA are described in [9].

The topology combines a PFC stage with an isolated DC/DC stage using only one semiconductor bridge and no internal DC-link. Because both the PFC and the DC/DC stage contain inductive elements which act as current sources, at least a small capacitor is required between them to limit the voltage spikes during switching. This is done using the active clamping snubber SA. The full circuit diagram can be seen in Fig 1. The advantage of this topology is using less semiconductors than in a comparable PFC and DC/DC arrangement. The drawback is that it requires large inductive elements, especially an oversized transformer which is not fully utilized. The 100Hz ripple from the output voltage cannot be fully eliminated by this circuit because of the absence of internal DC-link.

B. Simulation issues

Our task was to build a simulation model for this circuit using Matlab Simulink or a Pspice based simulation software. Because the current is determined by inductors on both the DC and the AC side of the inverter bridge, determining the voltage across the switches S1 – S4 is not straightforward. Building a fast structure change based model seemed to be feasible but because of the large number and the complicated nature of the possible switching states this approach was not pursued further. Approaches with snubber-based associated discrete circuit models [10] have also been tried. To obtain voltage values, the small capacitances parallel to the S2-S4 switches were included in the simulation with artificial leakage resistors. This way the time step had to be slowed down significantly, which has made debugging very complicated. This approach often caused non-convergent behaviour or numerical underflow problems. Artificially increasing the values of these time constants helped to some extent, but resulted in less realistic waveforms. As a final solution, a highly idealized model has been built.

2. Simplified Power Circuit Model

The inverter bridge and the SA switch has been omitted and replaced by an ideal state switch which only simulates 4 different states and only 3 possible voltage values: positive diagonal, negative diagonal or short circuit (2 possible pathways). The resulting model runs fast and gives realistic ideal current and voltage values for the larger dynamic components but does not directly generate separate current or voltage waveforms of IGBTs and diodes in S1-S4 or SA. The generation of waveforms and the actual conduction and switching loss calculation for all semiconductors has entirely been done via post-processing.

A. Bridge Model, Switching States

The simulated switching states are shown in Table I. From the snubber capacitors, only C_{SA} has been inclu-ded in the simulation by an integrator limited to positive values. The effects of C1 and C3 has been included in the post processing for switching loss calculation.

Table I. – Simulated switching states

State	S12	Short	S_1	S_2	S_3	S_4	S_A	V_{AC}	I_{SA}	V_{CE}
DC short	1	1	1	1	1	x	0	0	0	0
	0	1	1	x	1	1	0	0	0	0
Positive diagonal	1	0	1	1	0	0	1	V_{sa}	I_{DC}-I_{AC}	V_{sa}
Negative diagonal	0	0	0	0	1	1	1	-V_{sa}	I_{DC}+I_{AC}	V_{sa}

When a VCE short circuit is switched, the rectified mains voltage is applied to the L1 choke, and the I_{DC} current increases. When a diagonal configuration is switched, the SA branch diode starts conducting as described in the above-mentioned literature The SA semiconductor is switched on after a short time, and is left ON by a fixed width impulse. The SA branch voltage V_{SA} is then connected to the transformer. Its current increases from almost zero (the transformer magnetizing current) to about twice the current of the L1 choke. Meanwhile, the sign of the SA branch current I_{SA} reverses. Since the transformer primary current I_{AC} will be greater than the L1 choke current, when the SA semiconductor is switched off, the DC circuit short circuit will definitely occur, regardless of the switching state of the semiconductors in the bridge, simply due to the opening of the diodes. For this reason, this can be modeled as a single case. This has greatly simplified the simulation, as can be seen in the table above. The model of the inverter power circuit prepared in this way and supplemented with the capacitor C_{SA} is shown in Fig. 3.

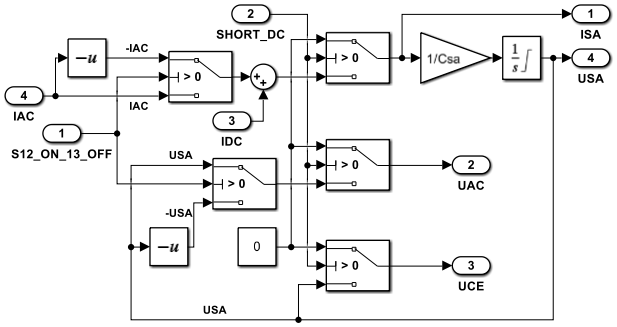

Fig. 3. Simulink model of the inverter bridge with active clamp

B. Timing and Control

The transformer is supplied with voltage for a fixed T_a time in each half-switching period, when the SA switch is on. So the current can only be controlled by changing the duration of the short-circuit state, resulting in a non-constant switching frequency. The voltage to which the C_{SA} capacitor is charged in steady state depends on T_a. It can be estimated by assuming a quasi-stationary state of operation, which means that the capacitor voltage V_{SA} after T_a time is the same as its initial value as in (3). Figure 4 was used to express this $V_{SA}(t)$ function in (1) It has three components. DC component Vout' is the output DC voltage reflected to the primary. If the initial capacitor voltage is different from Vout', a cosinusoidal component will be present. As $L_1 >> L_{LK}$, I_{DC} was treated as constant. Forcing I_{DC} to the LC circit causes a sinusoidal voltage on the Z_r characteristic impedance.

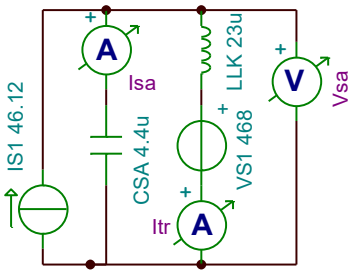

Fig. 4. Simplified circuit diagram of the active clamp LC circuit

$$V_{SA}(t) = V_{out}' + \left(V_{SA}(0) - V_{out}'\right)\cdot\cos(\omega_r t) + i_{DC} Z_r \sin(\omega_r t) \quad (1)$$

$$\omega_r = 1/\sqrt{L_{LK}\cdot C_{SA}},\ Z_r = \sqrt{\frac{L_{LK}}{C_{SA}}} \quad (2)$$

where (2) shows the self-resonant frequency and the characteristic impedance of the circuit. With the quasi-stationary condition, equation (3) can be expressed:

$$V_{SA}(0) = V_{SA}(T_a) = V_{out}' + \frac{i_{DC}\cdot Z_r \cdot \sin(\omega_r T_a)}{1-\cos(\omega_r T_a)} \quad (3)$$

In the actual device, T_a=14µs was used. With the component values of Fig. 4, initial V_{SA} is 600V at full load. Simulated waveforms of Fig. 4 using TINA TI are shown in Fig. 5. At t=0 the DC short circuit by the H-bridge is eliminated. A diagonal configuration is switched, causing the DC choke current to flow through the SA branch. It can be seen that the transformer primary current I_{tr} rises to double of the DC choke current.

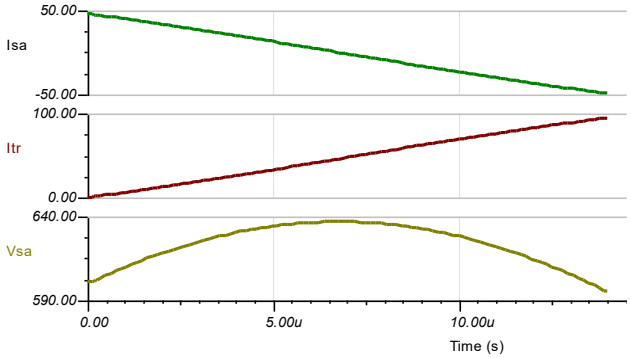

Fig. 5. Simulated waveforms of the SA active clamp for one T_a

As described before, individual semiconductors of the H-bridge were not simulated. Simplified control signals had to be generated for the model of Fig. 3. Each period is initiated by the current controller via *start_diagonal* signal. A simple timer-based unit was then used to generate two control signals as shown in Fig. 6:

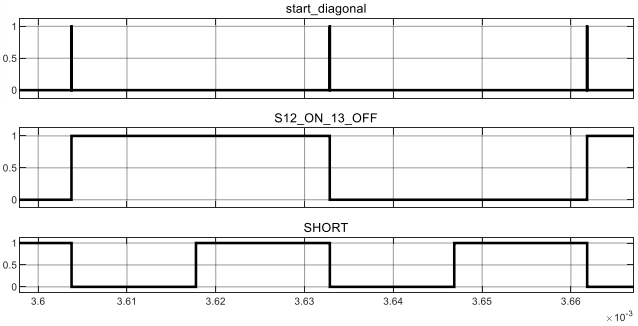

Fig. 6. Simplified control signals

Since the switching frequency is not constant, a simple comparator based peak current mode controller (PCMC) was created in the model to control the DC choke current. The current reference signal is proportional to the absolute value of the mains voltage. The controller keeps the H-bridge in a short circuit state until the input choke current i_{DC} reaches the current reference signal. Then the *start_diagonal* output of the current controller goes high and the next diagonal is switched for a T_a wide pulse.

Because the controller controls the peak current instead of the average, the current ripple also had to be determined. During the diagonal, the DC voltage $V_{CE}(t) = V_{SA}(t)$ for $0 < t < T_a$ as in (1) with the waveform of Fig. 5. This needs to be averaged for a T_a pulse. The average was calculated by substituting (3) into (1) and using the average $|\sin(\omega t)|_{av} = 2/\pi$ and the approximation $\tan(\omega_r T_a/2) \approx \omega_r T_a/2$. With the average of V_{CE} for T_a the calculation of the approximate ripple is possible as in (4).

$$\Delta I_L \approx \frac{|V_{grid}| - \left(V_{out}' + \frac{2}{\pi}\cdot i_{L1ref}\cdot\left(Z_r + \frac{2\cdot L_{LK}}{T_a}\right)\right)}{L_1}\cdot T_a \quad (4)$$

C. *Modelling of Reactive Components*

Modelling of the DC choke could be done using an ideal integrator, assuming that the ferrite core does not saturate. The value of the leakage inductance of the transformer adds to an external inductor, resulting in a net L_{LK} of 23µH. This has been included in the transformer model together with nonlinear magnetizing current calculation in the $I_m = p_1\cdot\psi + p_2\cdot\psi^k$ polynomial form. The constants p_1 p_2 and k were determined from laboratory measurement results on a transformer from a disassembled unit. The core cross section and turns ratio have been measured and used to calculate inductance B. This enabled core loss calculation during post processing. The transformer model with secondary is shown in Fig 7:

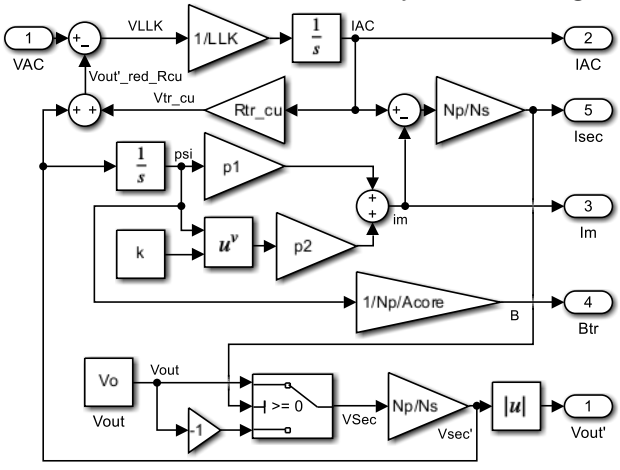

Fig. 7. Simulink model of the transformer and output rectifier.

3. Simulation Results with Simplified Model

Using the simplification methods described above, a Matlab Simulink model could be created which could be run for a full 20ms period of the utility grid. All values are in SI units. Due to the switching function based rectifier model of Fig. 6, the model can not be run with a

variable step solver. With a fixed time step of 10ns the 20ms model could run on a general purpose laptop in less than 1 minute. The simulation was run from 230Vrms 50Hz grid voltage to a 375V 20A load. Initial conditions of integrators have been set to reduce transients at the start of the simulation.

A. Bridge Model Waveforms

The resulting simulated waveforms for the inverter bridge and the SA active clamp circuit can be seen in Fig. 8. The first diagrams show the current of the SA capacitor and the transformer primary. The DC choke current and the operation of the current control can be seen in the middle diagrams. Voltages of the AC and DC side of the H bridge and of the SA capacitor are shown in the bottom diagrams.

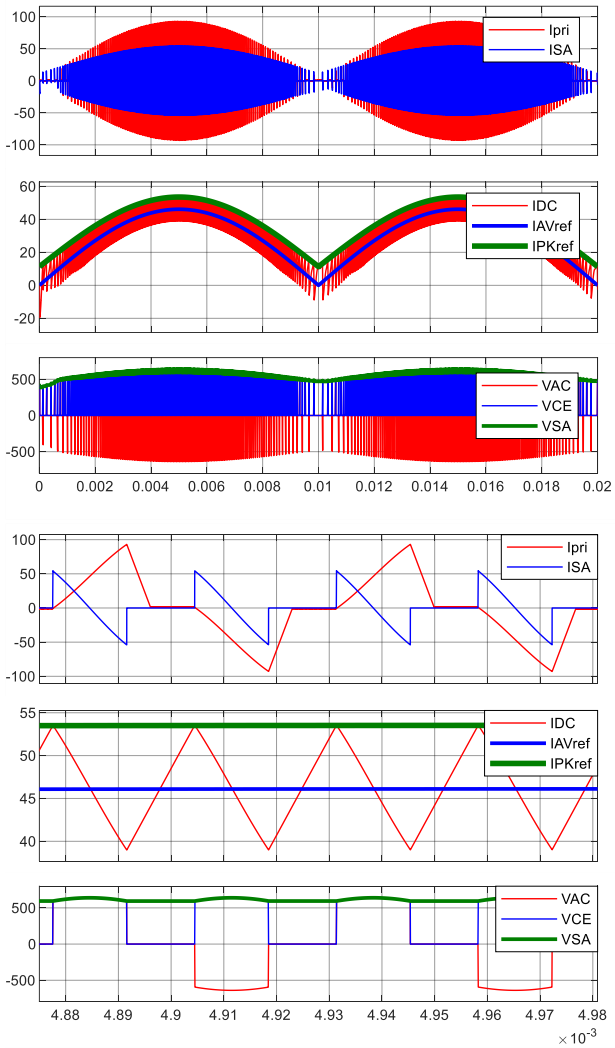

Fig. 8. Simulated waveforms of input side currents and voltages. Top: full 20ms. Bottom: magnified around peak grid voltage.

B. Transformer Waveforms

The recording of Fig. 9. shows signals that are relevant to the transformer. This figure shows even more clearly that the switching frequency is not constant, but very low around the zero crossings of the mains voltage and high at the peaks. By enlarging the waveform around the peak of the mains voltage, we can observe the magnetic induction. It is within saturation limits of the ferrite core.

By enlarging the current waveforms vertically, the magnetizing current waveform also becomes visible. Its initial value has been set such that the average value of the magnetizing current is zero. As expected, the primary current of the transformer is equal to the magnetizing current in the short-circuited state.

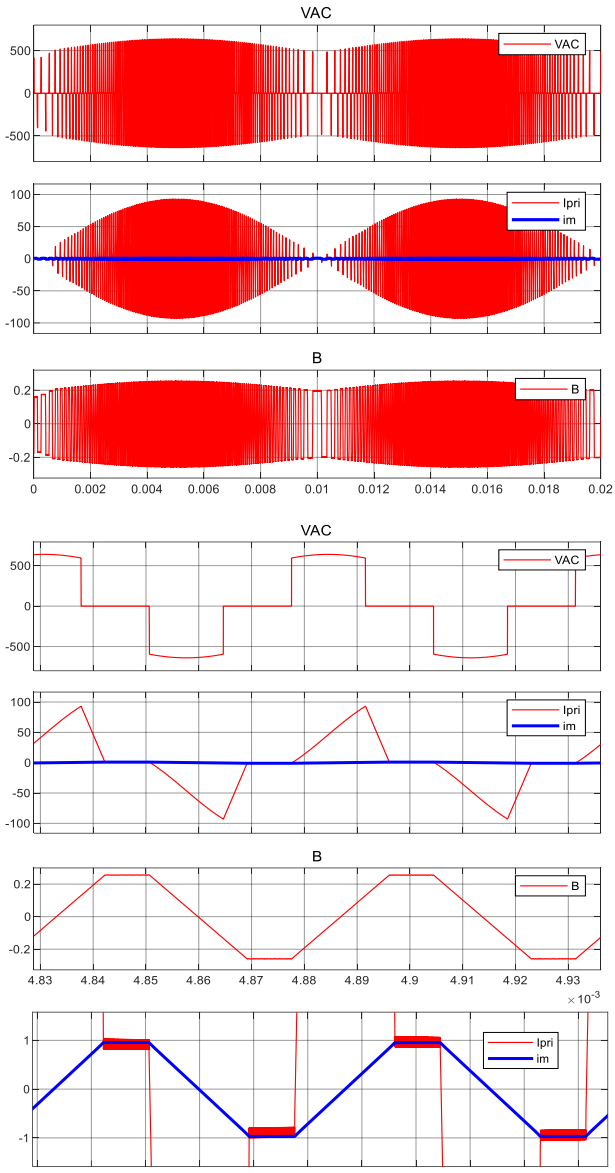

Fig. 9. Simulated waveforms from the transformer model. Top: full 20ms. Middle: magnified around peak grid voltage. Bottom: magnified magnetizing current waveform.

4. Loss Calculation from Simulation

After the simulation has been run in Simulink, all waveforms required for post-processing have been exported to work-space and saved to a 200MB MAT file. Processing has been done via MATLAB scripts.

A. Inductive Component Losses

Losses for the DC choke L_1, the additional resonant inductor part of L_{LK} and for the transformer were calculated using similar methodology. Resistive copper losses were calculated from RMS currents which were calculated from the full waveforms. Because all inductive components were manufactured using Litz wire, and the switching frequency is below 20kHz, the Skin effect was

not included in the calculation. Core losses were calculated from simulated voltage waveforms using the extended Steinmetz's equation for nonlinear excitation (5) from [11]. The time integral of the voltage divided by the number of turns and the iron cross-section gives the time function of the magnetic induction. To determine the core loss, the effective value, the absolute mean value and the average magnetic induction change are required. These were generated by MATLAB script. Inductive component losses were in good agreement with losses calculated from stored oscilloscope measurements of voltages and currents.

$$P_{core} = V_{core} \cdot \left(\frac{1.234}{4.863^{\alpha}} \cdot K \cdot \left(\frac{dB}{dt} \right)_{RMS}^{(1.86\alpha - 2)} \cdot \left| \frac{dB}{dt} \right|_{AVG}^{(2-0.86\alpha)} \cdot \Delta B_{AVG}^{(\beta - \alpha)} \right) \quad (4)$$

B. Waveform Generation for Switching Transistors

Due to the operation of the circuit and the choice of fixed switching times, the waveforms and the losses of the upper two IGBT-diode pairs are not the same as those of the lower half of the bridge. The individual fixed switching delays were read from the original control software of the device. The complicated shapes of the current waveforms of individual IGBTs were generated by masking and adding parts of the I_{DC} I_{AC} and I_{SA} current waveforms occurring in the individual switching states. It was assumed that the two diagonals of the H bridge generate identical losses. It was sufficient to examine the losses of the S1-S2 IGBTs and the S3-S4 diodes in a period where the diagonal was provided by the S1 - S2 IGBTs. The resulting waveforms were compared with the waveforms measured on the real system, thereby validating the simulation. The current waveforms compiled during the post-processing are shown in Fig. 10 for the high side and in Fig. 11 for the low side. The waveforms for a full grid period are shown on the left, and magnified versions around the peak are shown on the right. The actual switching sequences are not detailed due to space reasons.

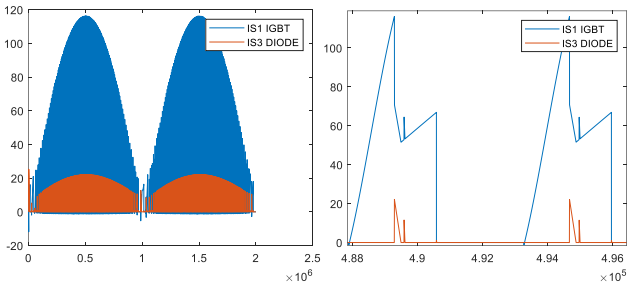

Fig. 10. Simulated high side semiconductor current waveforms

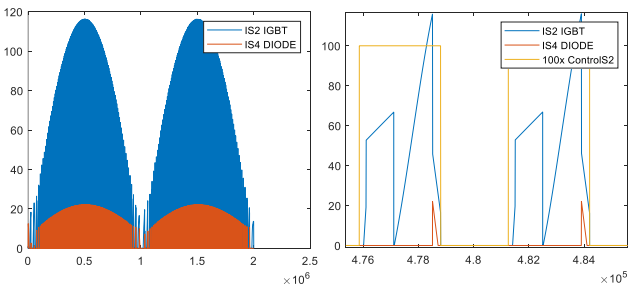

Fig. 11. Simulated low side semiconductor current waveforms

C. Semiconductor Losses

Diodes and IGBTs were modelled using piecewise linear approximation for conduction loss calculation. An initial voltage drop and dynamic resistance value has been determined from the forward characteristics of each semiconductor for a typical operating temperature. Conduction losses could then be calculated from the current waveforms and averaged for a full grid period. Switching losses for IGBTs were calculated for hard switching operations using the formula (5) from [12] where for IGBTs Ki≈1, Kv≈1.3.

$$E_{sw} = E_{swref} \cdot \left(\frac{I}{I_{ref}} \right)^{Ki} \cdot \left(\frac{V}{V_{ref}} \right)^{Kv} \quad (5)$$

IGBT gate signals were generated from control signals saved from the Simulink simulation. By shifting the gate signal by one sample and performing XOR operation with the original vector and then masking the turn-on and the turn-off pulse (AND operation), vectors could be created that have a value of 1 for one sample during each turn-off or turn-on. These were used for masking the calculated energy vectors from (5) in the post processing script. Power dissipation could be calculated by summing the elements of the resulting vector and dividing by simulation duration. This hard switching calculation method was used for the switch-off of SA and also for the high side S1 and S3 switches. This was the case because calculations have shown that with the slow IGBTs used in the circuit, the parallel snubber capacitors of S1 and S3 are insufficient to significantly reduce the switching losses. ON-switching can be considered ZVS for the SA, S1, and S3. The low side S2 and S4 switches turn on and off via ZVS for high currents, but have switch-on losses for small currents insufficient to charge the capacitors parallel to S1 or S3 during the available fixed time. This also applies to the turn-off of SA. These additional losses are only present near zero crossings.

D. Reverse Recovery Losses

Apart from conduction losses, secondary rectifiers also have significant switching losses due to reverse recovery and have snubbers with additional losses. Reverse recovery energy was calculated using the approximation (6) where $V_{rr} \approx 2V_{out}$ but Q_{rr} is a function of peak current and the slope of the current. The latter was calculated from V_{out} and L_{LK} and was also checked by measurements on the actual hardware. Dependence of Q_{rr} from the peak current was checked in the datasheet and approximated via square root function.

$$E_{rr} = 0.8 \cdot Q_{rr} \cdot V_{rr} \quad (6)$$

E. Loss Calculation Summary

The original simulation was performed without taking into account most of the losses. The problem is that power lost in one stage of the converter flows through all preceding stages, generating additional losses. To

compensate for this, a proportional correction for current increase has been added to preceding stages. Voltage drop also results in increased duty ratio which – for this type of converter – also increases the switching frequency. After compensating for these effects, the results already came close to results obtained from oscilloscope measurements on individual IGBTs in actual hardware. The distribution of losses between the components can be seen in Fig. 12.

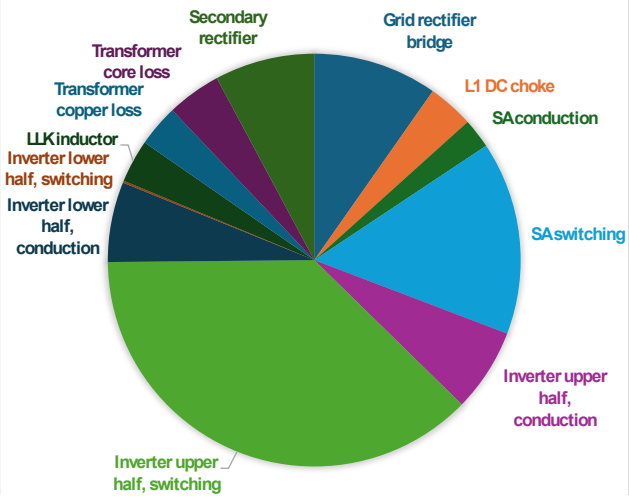

Fig. 12. Distribution of losses calculated from simulation

The losses calculated so far were in agreement with expectations based on oscilloscope measurements. Fig 12 shows that the inverter upper half switching losses are quite significant. This could easily be reduced by increasing the parallel capacitors and adjusting timing. However, the total efficiency was calculated to be 91.43% while the actual hardware has an efficiency below 87%, meaning that ca 420W of losses are unaccounted for. It is obvious that several loss components were not taken into account. Losses from capacitors (especially electrolytics on the output), wiring and input EMC filter could not be easily measured but probably in the range of 30..50W total and the auxiliary power supply driving the gate drivers, controller and relays could have a similar consumption, but a total of 420W is not expected from these. However, comparing waveforms of Fig. 10 and 11 with oscilloscope measurements on an actual device have shown that overvoltages and high frequency oscillations occour in the wiring connecting S1, S3 and SA IGBTs which is probably caused by high inductance of the wiring. Losses caused by this were not quantified, but could easily be hundreds of watts. This could be alleviated by decreasing inductances via better placement of semiconductors and using busbars instead of wiring. Improvements in switching losses are also possible by replacing IGBTs with modern MOSFETS.

7. Conclusion

In this paper it was shown that power circuits using ZVS and small time constant snubbers can be simulated in a two-step process. A highly simplified ideal model can be used to generate waveforms of large dynamic components. Post-processing can then be used to generate the rest of the waveforms and to include losses. Comparison of computer simulation results with oscilloscope measurements could help to identify anomalies and sources of losses in an existing design, helping in improvements.

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