International Conference on Renewable Energies and Power Quality (ICREPQ'20)

A Programmable Source Based on Multi-level Buck EIE Inverter Connected to a Power Factor Correction Stage Composed by a Single-phase Hybrid Rectifier

G. N. Souza[1], D. B. Rodrigues[1], G. B. de Lima[2], L.C.G. de Freitas [2], A.J.P. Rosentino Junior[1], M.R.M. Castillo[1], F.A.M. Moura[1] , R.R. de Lima[1], W.B. de Melo[1] and P.V. Parreira[1]

Electrical Engineering Department, [1]Universidade Federal do Triângulo Mineiro, Uberaba - Minas Gerais, Brazil
Electrical Engineering Faculty, [2]Universidade Federal de Uberlândia, Uberlândia - Minas Gerais, Brazil.

I - Introduction

Recently, the role of photovoltaic (PV) energy in the utility grid has increased with the sustained growth of PV technology and continuous decreases in the Price of PV products. Although PV energy is an abundant energy source, PV output power fluctuates according to the environmental conditions. This fluctuations cause negative effect on the power quality and reliability of a PV system.
After the electrical voltage generation, many devices adjust the voltage level through the use of DC-DC converters. The most common voltage sources are linear and switched sources. Linear sources are widely used because of their high dynamic response, constructive simplicity and relatively low cost . They are composed of semiconductor devices that operate in the linear region, besides having a transformer for galvanic isolation and a variable resistor. However, they have some undesirable characteristics, such as low efficiency, high weight and volume of passive components compared to the switched sources and the size and losses of the transformer operating at the power supply frequency (low frequency) .
One type of programmable source that has tremendous versatility and quality coupled with its ease of construction is the Buck EIE topology-based converter. Such devices are capable of individually controlling the inductor current as well as the output capacitor voltage. that make up your circuit. In this way, they can make the output voltage practically immune to load variations
The present work will address the use of Buck EIE converters associated with a power factor pre-regulation stage and harmonic current distortion involving a hybrid rectifier circuit, The main benefit provided by hybrid rectifiers is the combination of weight and volume reduction from high frequency switched converters with the simplicity and robustness of uncontrolled diode converters.

.

II – Methodology

The Single Ended Primary Inductance Converter (SEPIC) converter was chosen because it presents current source behavior, that is, the imposition of the desired current waveform does not depend strongly on the static gain of the converter. Although in the present work such a converter acts only as a voltage depressor, it has the versatility of operating as a voltage elevator as well. The inductor L1 of the Sepic converter will be allocated before the rectifier bridge, however, all equation will be done as if it were allocated in the position shown in Figure 1, in order to simplify the modelling.

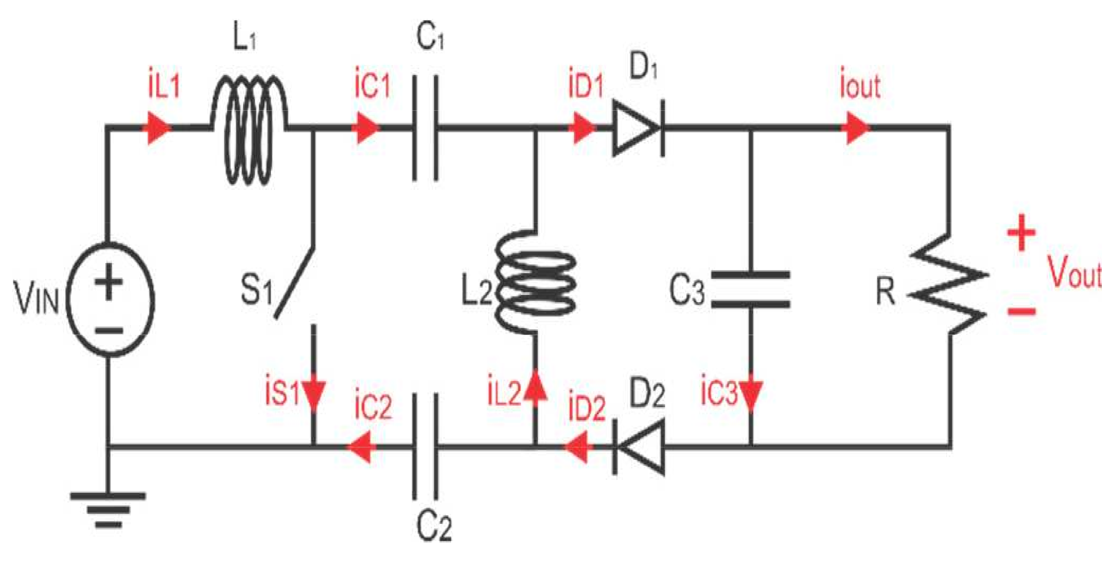

Fig. 1. Sepic Converter

A Buck EIE converter is capable of supplying a load connected to it with a single polarity voltage. In order to meet one of the proposed objectives of this work, which is to supply the load with a voltage that follows a pre-established voltage reference that can have its value varied rapidly, whether of continuous or alternating nature, it is necessary to use two converters.
The arrangement formed by the set of two Buck EIE converters form the Buck EIE inverter. The Buck EIE converter connected to the uncontrolled rectifier will be responsible for increasing the voltage in the load, while the converter connected to the switched rectifier will be in charge of decaying the voltage supplied to the load.
The design of the single-phase hybrid rectifier and Buck EIE inverter was based on the desired input and output voltage of each step, obeying the ripple levels acceptable. The complete circuit described in this paper is illustrated in Figure 2.

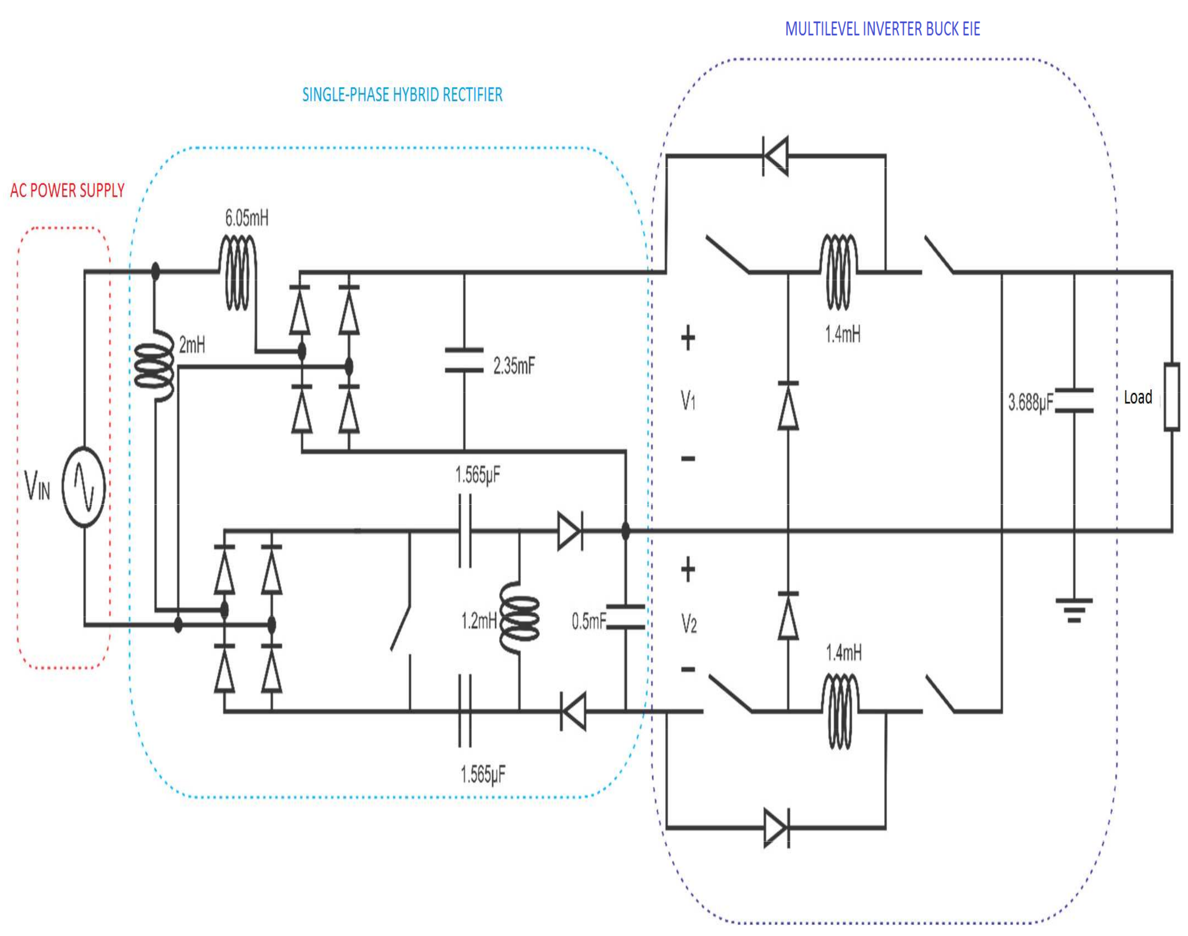

Fig. 2. Buck EIE multi-level inverter connected to a PFC stage consisting of a single phase hybrid rectifier

Control Estrategy

The control of the Sepic converter is performed using the circuit shown in Figure 3. The reference current (I_{ref}) is generated using a Phase-Locked Loop (PLL), which generates a moored current reference (in phase) with the input supply voltage. This signal is multiplied by the output signal of a PI controller which is responsible for minimizing the error between sensed ($V_{out\ (ret\text{-}2)}$) and reference ($V_{out\ (ret\text{-}1)}$) output voltages. Then, the resulting signal is multiplied by the set reference current (i_{ref}) and shortly thereafter, it is compared to the absorbed current from the mains (i_{in}).

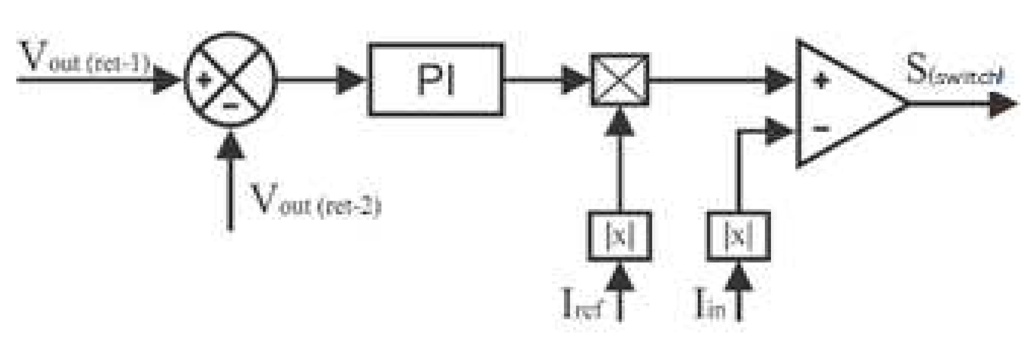

Fig. 3. Sepic converter control circuit.

IV – Results

The figure 4 shows the output voltage of the Buck EIE invertir as well as the voltages at the circuit outputs rectifiers. The proposed output reference voltage was a 60 Hz sinusoid and 100 Volts peak. The output voltage represented by the red curve is completely according to the established reference parameters.

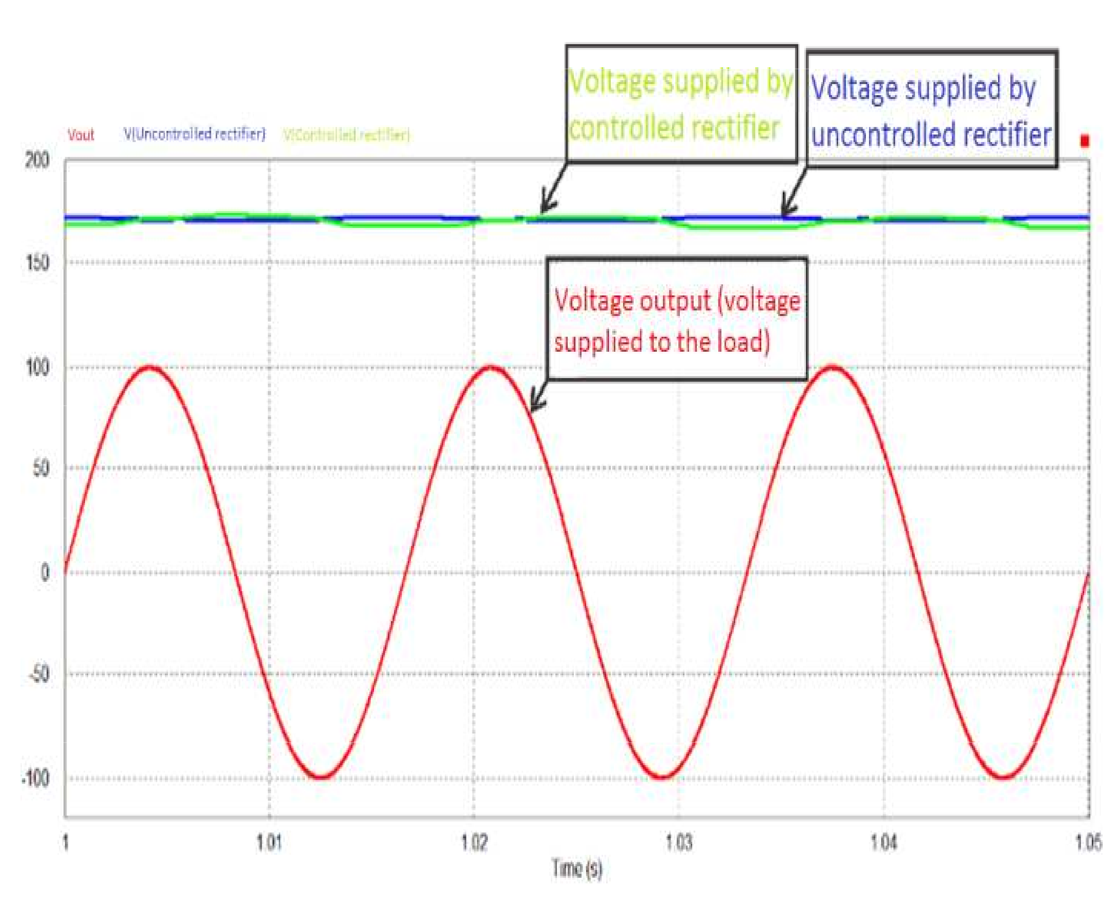

Fig. 4. . Waveforms obtained by simulating the voltage supplied load, the output voltage of the controlled rectifier and the non- controlled.

The Buck EIE inverter is capable of generating output voltages of various shapes and frequencies. Figure 5 shows the resulting output voltage for voltage reference at 20Hz with 100 peak voltage.

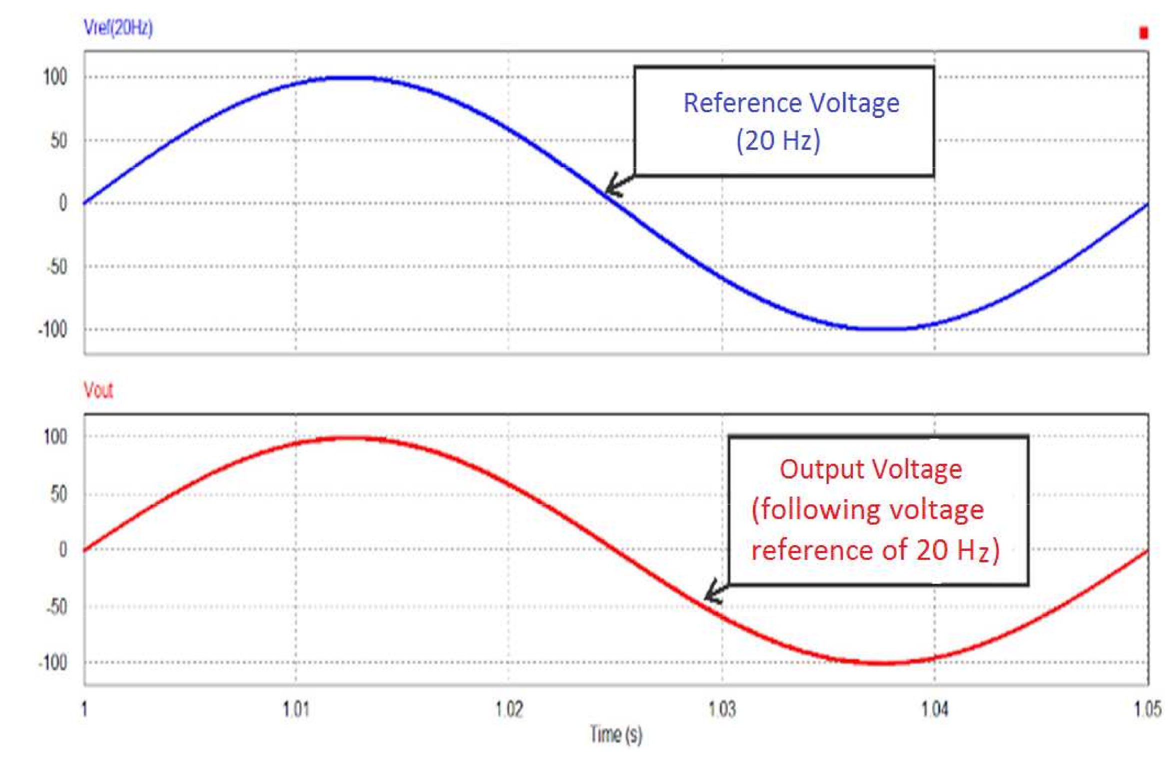

Fig. 5. Frequency inverter following 20 Hz sine reference voltage (simulated waveforms).

This inverter topology becomes very useful for studies in the field of power quality, especially when the scope of study is on the presence and effects caused by the presence of harmonics in the power grid. Figure 6 shows the inverter following a voltage reference composed of sine harmonics, specified in Table I.

Table I. - Characteristic of harmonic components present in the established voltage reference

Harmonic Order	Frequency (Hz)	Peak Voltage (V)
Fundamental	60	70
Third	180	30
Fifth	300	50
Seventh	420	10

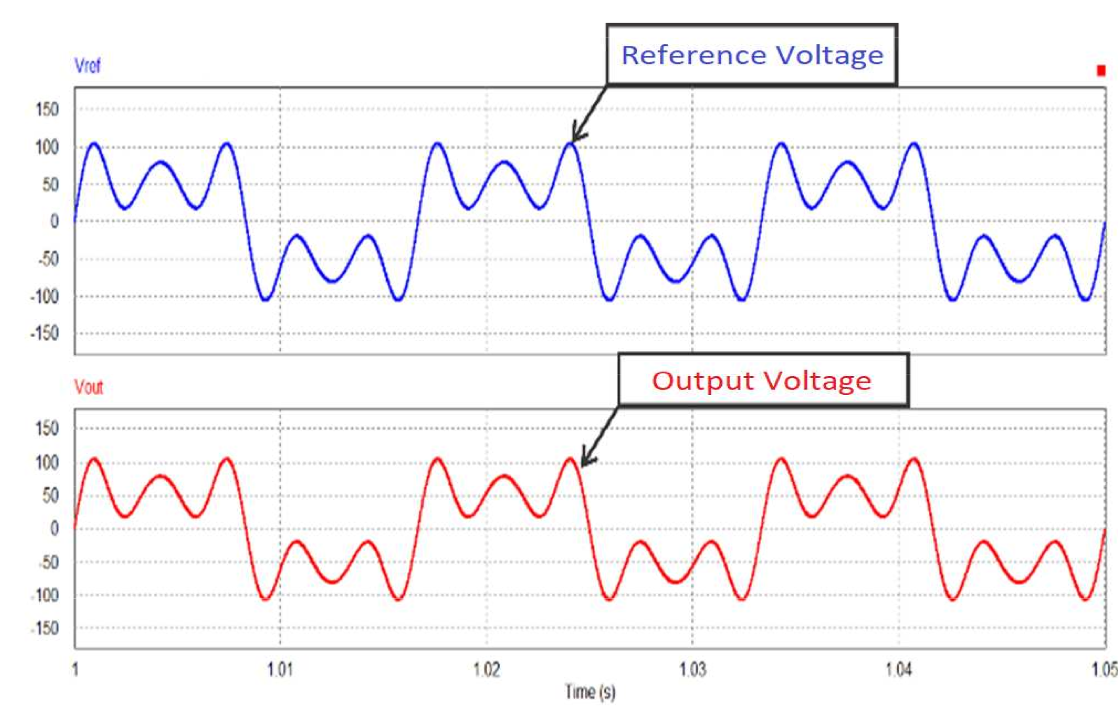

Fig. 6. Frequency inverter following reference voltage with presence of third, fifth and seventh order harmonics

VI - Conclusions

A power factor correction stage proposal based on the use of a single phase hybrid rectifier to supply a Buck EIE multi-level inverter was presented. The PFC stage is performed by the association of a controlled rectifier (Sepic) and an uncontrolled one, which is responsible for increasing the overall structure yield. This circuit has as its main function to ensure that the input voltage and current are in phase, resulting in a high power factor (very close to the unit). In addition, it is desired that the output voltages of the hybrid rectifier be kept at a constant value, and that the input current waveform presents low harmonic distortion.
The results obtained through simulations performed in the PSIM v.11 software were very satisfactory, since the Buck EIE inverter provided the desired voltage for the load and the current drained from the mains, besides being in phase with the voltage, presented low DHT.

This work was supported by:

CAPES CNPq