404

21th International Conference on Renewable Energies and Power Quality (ICREPQ'23)
Madrid (Spain), 24th to 26th May 2023
Renewable Energy and Power Quality Journal (RE&PQJ)
ISSN 2172-038 X, Volume No.21, July 2023

Performance Evaluation of Grid Connected T-Type Multilevel Inverters

Kevin ACADINE[1], Augustin MPANDA[2] and Ahmed EL HAJJAJI[1]
[1]MIS Lab, University of Picardy, France
[2]SYMADE, UniLaSalle Amiens

Introduction : T-Type structure requires fewer power devices than Neutral-Point-Clamped and Flying-Capacitor inverters for the same power level. The performance evaluation of two grid-connected T-Type inverters, 3L and 5L, is carried out. The DC bus voltage is considered perfect. The dynamic behaviour of this association is presented in the form of mathematical equations. A PI controller is used to control the d- axis and q-axis currents respectively. The sine Pulse Width Modulation (PWM) technique is used to control the MOSFET switches. The simulation of the complete system has been performed on MATLAB/Simulink and is presented at the end.

▪ Dynamic model of grid-tied T-Type inverters

Assuming the grid balancing : $v_{g,a}+v_{g,b}+v_{g,c}=0$. The dynamic model of grid-tied T-Type inverters can be made. We denote $x=[a,b,c]^T$ .According to Kirchhoff's voltage law:

$$L\frac{d\,i_{i,x}}{dt} = -R\,i_{i,x} + v_{i,x\_O} + v_{O\_N} - v_{g,x}$$

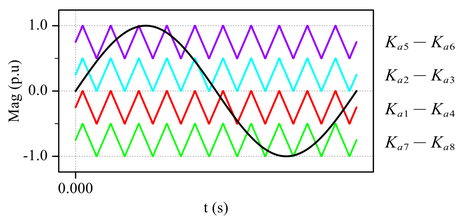
The structure of the inverter is scalable to higher levels, as well as the mathematical model. Below is the complete mathematical model of the T-Type 5L inverter connected to the grid:

$$[Li_a^{\cdot} \quad Li_b^{\cdot} \quad Li_c^{\cdot} \quad Cv_{C4}^{\cdot} \quad Cv_{C3}^{\cdot} \quad Cv_{C2}^{\cdot} \quad Cv_{C1}^{\cdot}]^T = A_5\,X_5 + B_5\,U_5$$

$$A_5 = \begin{bmatrix} -R & 0 & 0 & M_aS_{a4} & M_aS_{a3} & M_aS_{a1} & M_aS_{a0} \\ 0 & -R & 0 & M_bS_{b4} & M_bS_{b3} & M_bS_{b1} & M_bS_{b0} \\ 0 & 0 & -R & M_cS_{c4} & M_cS_{c3} & M_cS_{c1} & M_cS_{c0} \\ -S_{a4} & -S_{b4} & -S_{c4} & 0 & 0 & 0 & 0 \\ -S_{a43} & -S_{b43} & -S_{c43} & 0 & 0 & 0 & 0 \\ S_{a10} & S_{b10} & S_{c10} & 0 & 0 & 0 & 0 \\ S_{a0} & S_{b0} & S_{c0} & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$B_5 = \begin{bmatrix} -2/3 & 1/3 & 1/3 & 0 \\ 1/3 & -2/3 & 1/3 & 0 \\ 1/3 & 1/3 & -2/3 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \end{bmatrix};\ X_5 = \begin{bmatrix} i_{i,a} \\ i_{i,b} \\ i_{i,c} \\ v_{C4} \\ v_{C3} \\ v_{C2} \\ v_{C1} \end{bmatrix};\ U_5 = \begin{bmatrix} v_{g,a} \\ v_{g,b} \\ v_{g,b} \\ i_{dc1} \end{bmatrix};$$

▪ Modulation Technique



The modulation technique used is a classical Level Shifted PWM, where the carriers are shifted in amplitude. Each carrier corresponds to a switching arm and a voltage level of the inverter. It satisfies the v_{ck} balancing of three-level T-Type structures quite well. At the higher level, the switching states increase and have more degrees of "freedom" - due to the increase of switches - which is an advantage but also a disadvantage. One of the main drawback is the unbalanced voltage of the capacitors. The unbalance shows a non-zero current at each capacitor:

$$i_{Ck}\,dt = C_k\left(V_{Ck} - \frac{V_{dc1}}{n-1}\right)$$

▪ T-Type inverter control strategy

The PI linear controller is used to control the d- and q-axis currents of the inverters. The active and reactive powers injected by the power inverters are proportional to d- and q-axis currents, respectively.

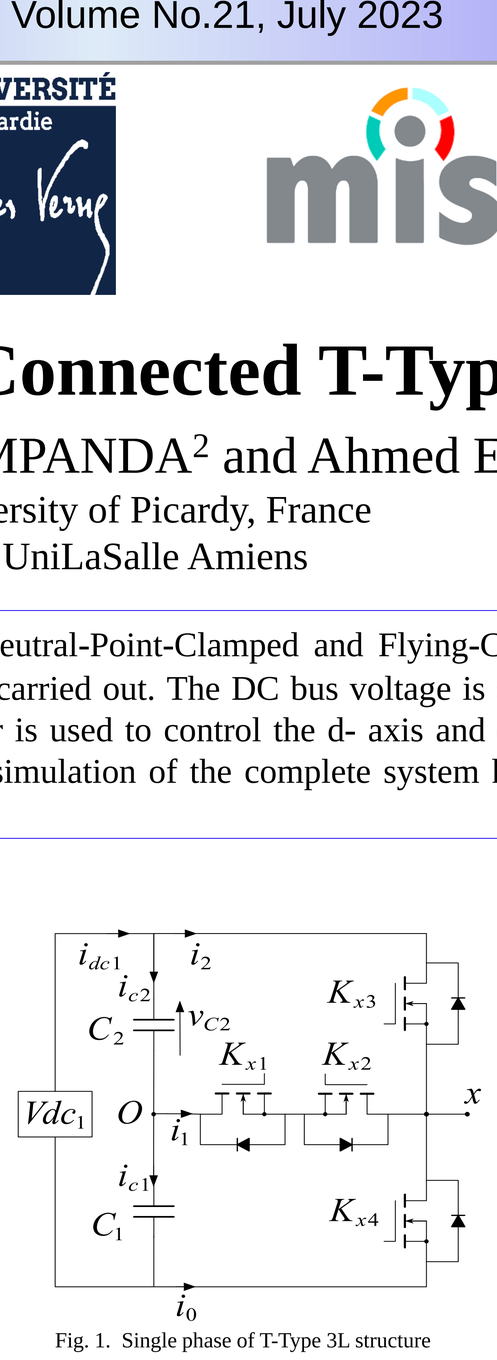


Fig. 1. Single phase of T-Type 3L structure

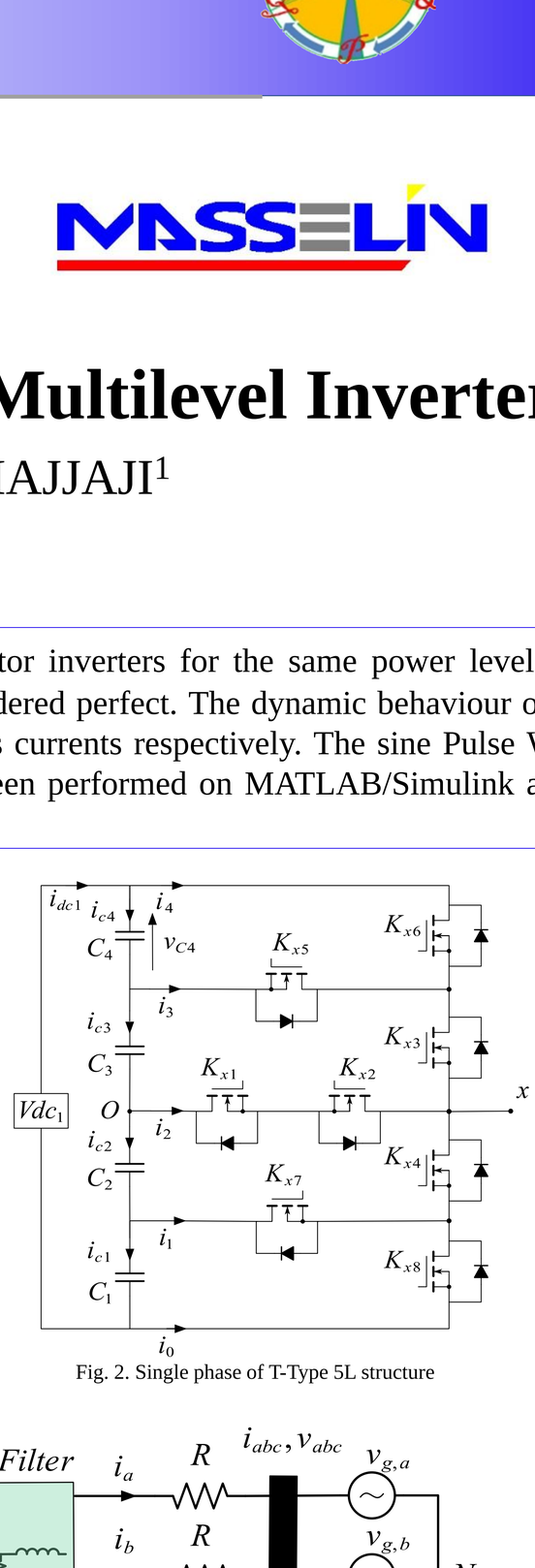


Fig. 2. Single phase of T-Type 5L structure

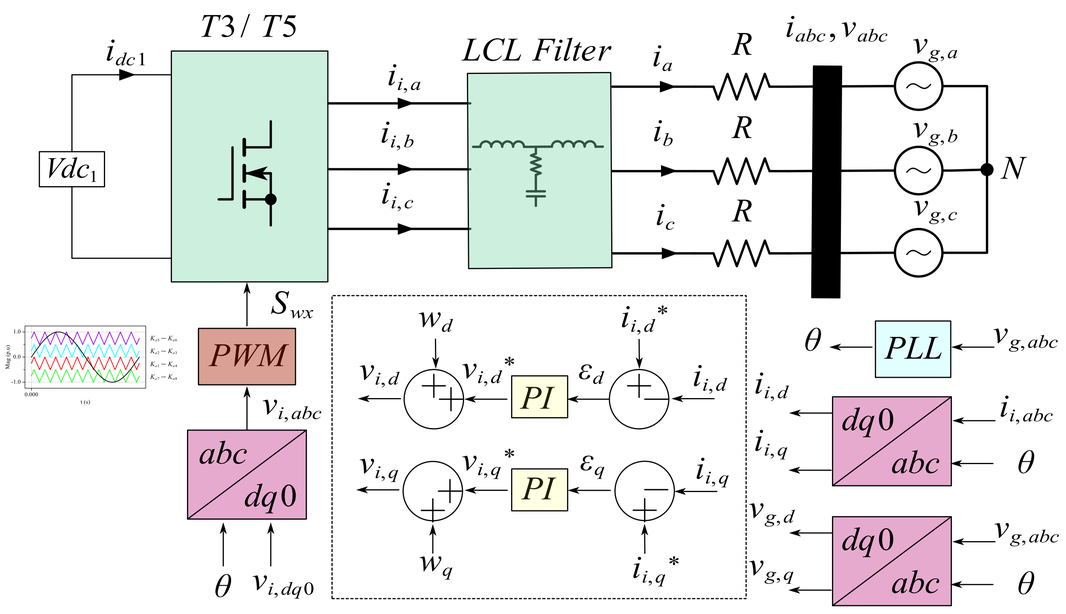


Fig. 3. Grid connected T-Type inverter, PI Controller

➢ Simulation results

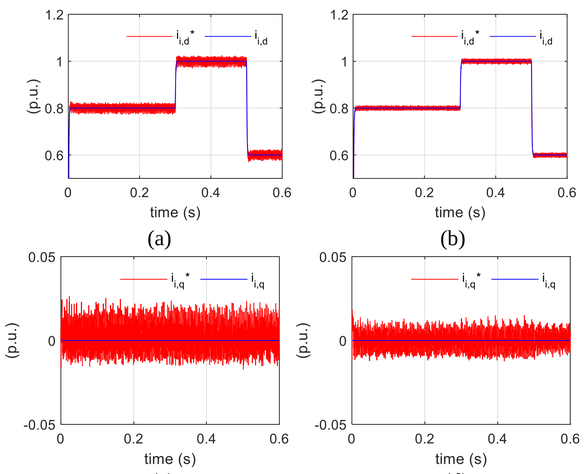


Fig. 4. T3: d-axis (a) and q-axis currents (c) ; T5: d-axis (b) and q-axis currents

Fig. 5. THD of phase a current (Before Filter), T3 (a) and T5 (b), respectively

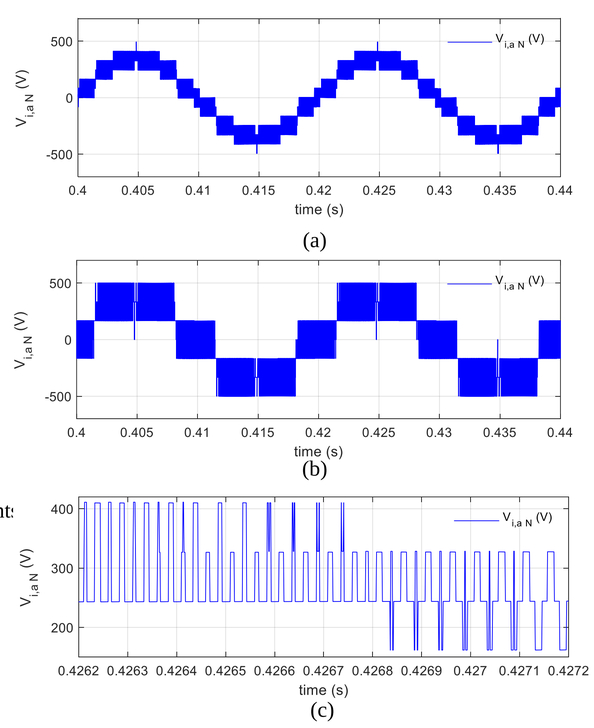


Fig. 6. T3: Inverter output voltage (a) ; T5 : Inverter output voltage (b) ; T5 : Inverter output voltage (1 ms) (c)

Conclusion : This study compares the performance of grid-tied T-Type three-level and five-level inverters utilizing a closed-loop strategy. The PI linear controller is employed for d- and q-axis current reference tracking, and the analysis is conducted without considering any disturbances. The simulation results indicate that both inverter structures show satisfactory dynamic performance, with the T5 inverter structure exhibiting superior signal quality concerning AC side current and voltage total harmonic distortion. This paper confirms the validity of the T-type inverter grid-connected mathematical model, and it also facilitates the identification of potential variables that are susceptible to intrinsic imbalance. The classic sine Pulse Width Modulation technique was utilized to control the MOSFET switches, under the assumption of perfectly balanced capacitor voltages. However, to overcome the issue of imbalanced DC-side capacitor voltages, a forthcoming article will employ a Space Vector Pulse Width Modulation algorithm. The latter will be integrated with closed loop strategies.